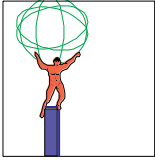


U.S. ATLAS



Silicon Subsystem

M. G. D. Gilchriese

July 21, 1999



Deliverables - Goals

1.1.1 Pixel System(Preliminary)

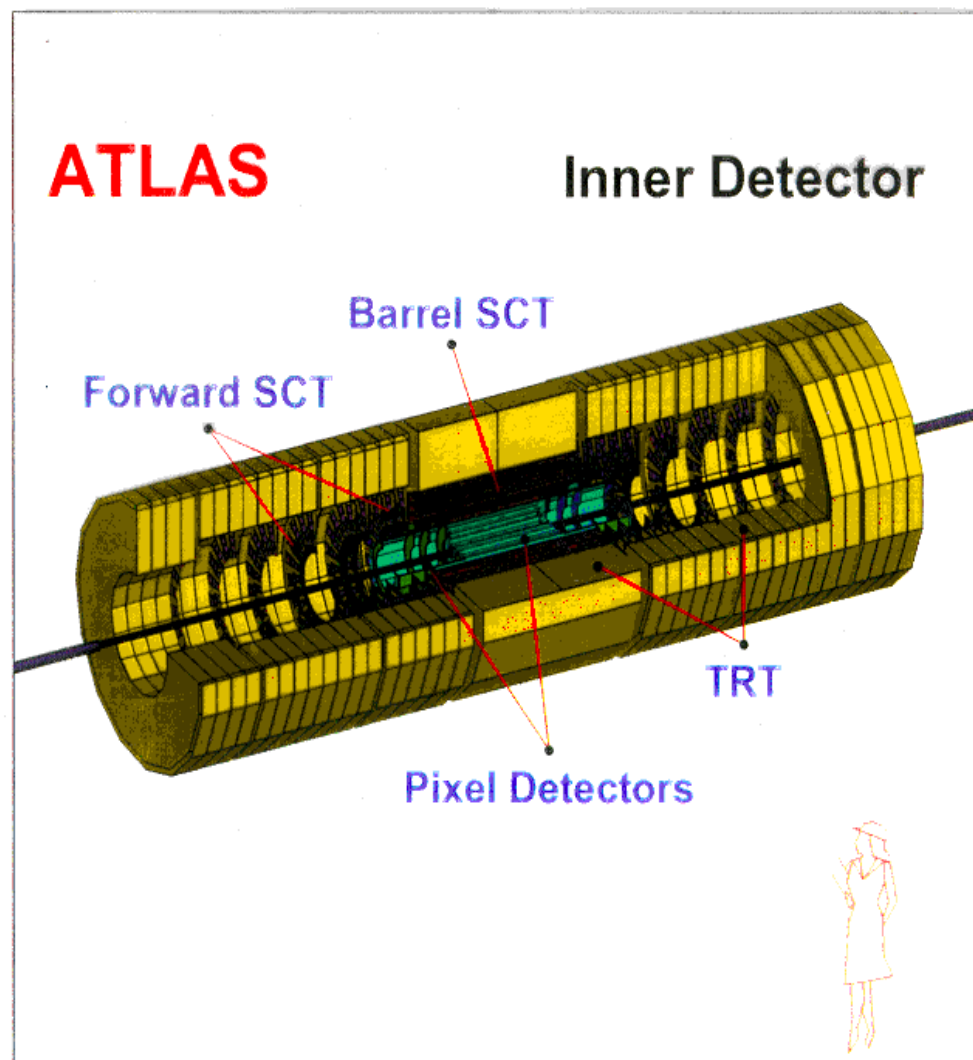
- ◆ 1.1.1.1 Mechanics - design, assemble and install disk system and outer frame(100%)
- ◆ 1.1.1.2 Sensors - design(30%) + procure and test 250 wafers(20%)
- ◆ 1.1.1.3 Electronics - design(40%)+procure and test 8500 ICs(25%)
- ◆ 1.1.1.4 Hybrids - design, fabricate, test(25%)
- ◆ 1.1.1.5 Modules - design, fabricate and test disk modules(100%)

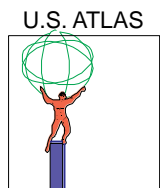
1.1.2 Silicon Strip System

- ◆ 1.1.2.1 Electronics - design(25%)+procure and test ICs(50%)
- ◆ 1.1.2.2 Hybrids - barrel design (100%) + procure all needed for US modules
- ◆ 1.1.2.3 Modules - deliver 670 modules(15%)

1.1.3 Read-Out Drivers

- ◆ Test beam support - pixel support boards(3 generations), DSP modules(50) + preprototype RODS(16)
- ◆ Design, fabricate, test and install pixel (100%) and SCT(75%) RODs.





Who Is Doing What

ALB LBL UCSC UNM UOK UW OSU

1.1.1 Pixels

1.1.1.1 Mechanics

X

1.1.1.2 Sensors

X

1.1.1.3 Electronics

X

X

1.1.1.4 Hybrids

X

X

X

1.1.1.5 Modules

X

X

X

X

X

1.1.2 Silicon Strips

1.1.2.1 IC Electronics

X

X

1.1.2.2 Hybrids

X

X

1.1.2.3 Modules

X

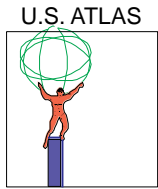
X

1.1.3 RODs

X

ALB = SUNY, Albany
 LBL = Lawrence Berkeley National Lab
 UCSC = UC Santa Cruz

UNM = U. of New Mexico
 UOK = U. of Oklahoma
 UW = U. of Wisconsin
 OSU = Ohio State



Read-Out Drivers

- **Test beam support**

- ◆ Digital Signal Processor(DSP) modules for both pixel and silicon strip laboratory and test beam measurement.

- ▲ Ongoing for last three years.
- ▲ Extensively made available to collaboration

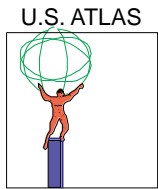
- ◆ **Pixel support**

- ▲ First generation test chips supported by custom test boards - this work is complete
- ▲ Custom VME boards for full-scale prototype pixel electronics essentially complete(upgrades only)
- ▲ These boards are part of dedicated, PC-based test system developed. Under high demand as standard. Replicated >10 places.

- ◆ Overall - very successful

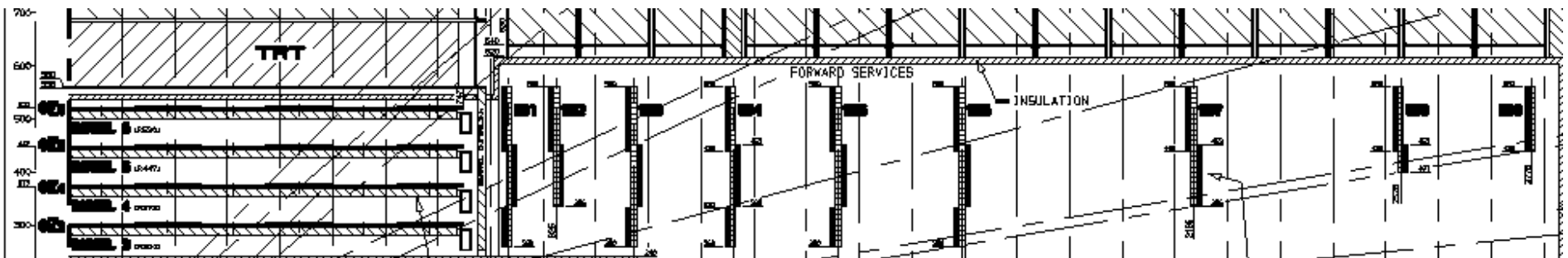
- **Prototype ROD**

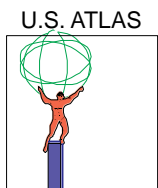
- ◆ Design underway
- ◆ First boards in February 1999
- ◆ Community test/system test spring->summer 1999.
- ◆ This will include prototypes of all interfaces - full “crate system”



Semiconductor Tracker(SCT)

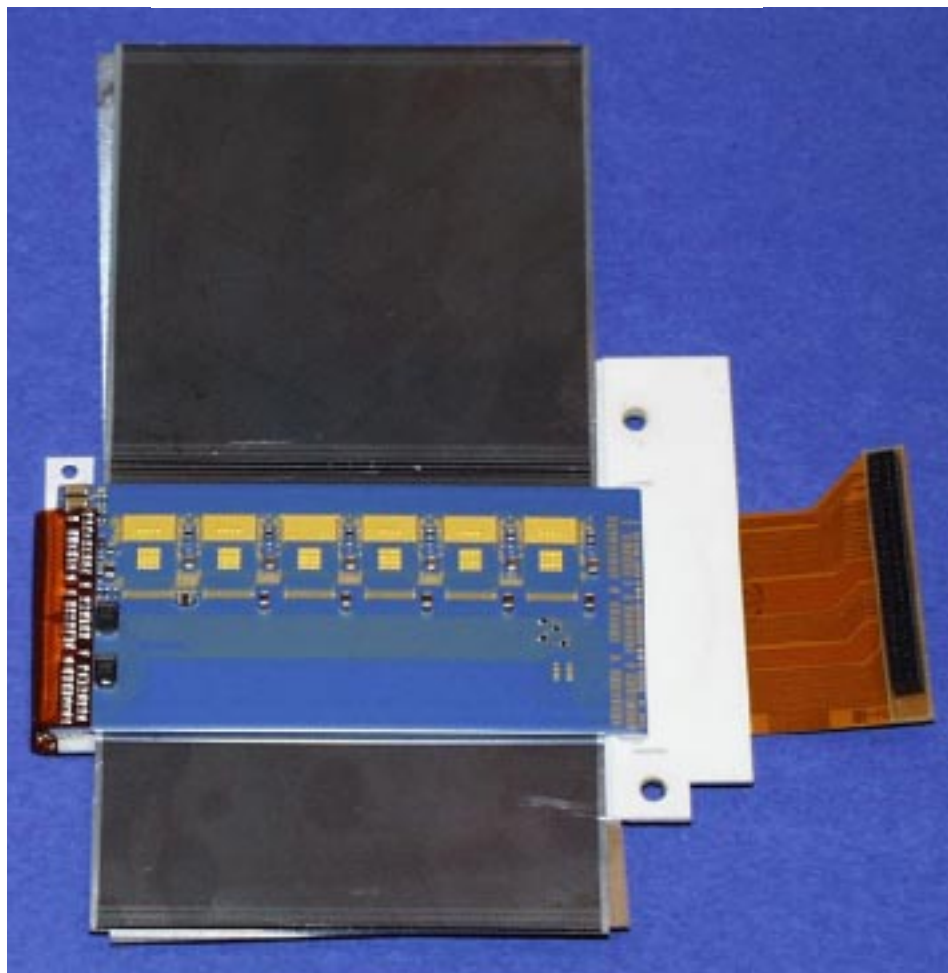
- Lots of silicon
 - ◆ About 60 m²
 - ◆ About 6 million channels
 - ◆ Single-sided, p-on-n detectors bonded back-to-back to provide small angle stereo => modules
- Only US work in this talk
 - ◆ Electronics
 - ◆ Modules
- Not U.S.
 - ◆ Detectors - passed Final Design Review - OK so far but production still ahead
 - ◆ Mechanics - conceptual->preliminary design phase. Needs work.



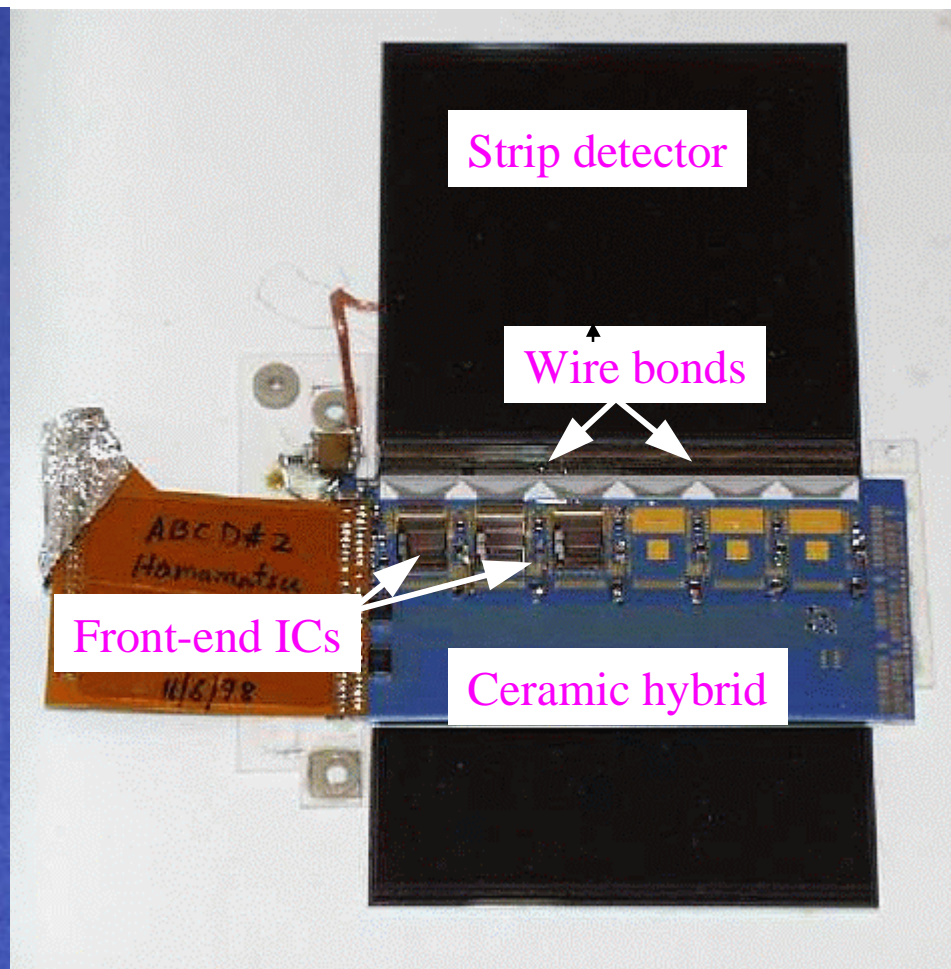


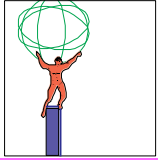
Barrel Silicon Strip Modules

Double-sided dummy module



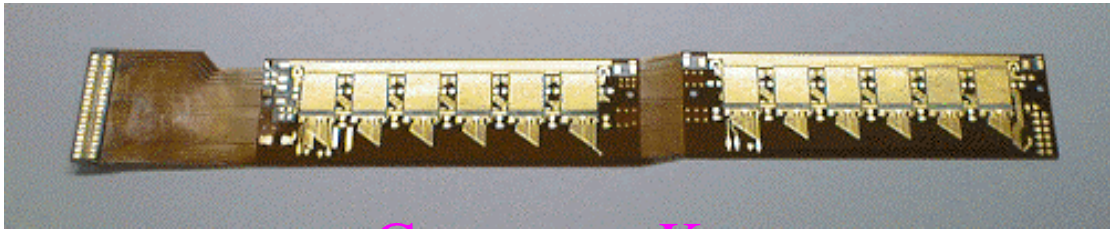
Single-sided active module



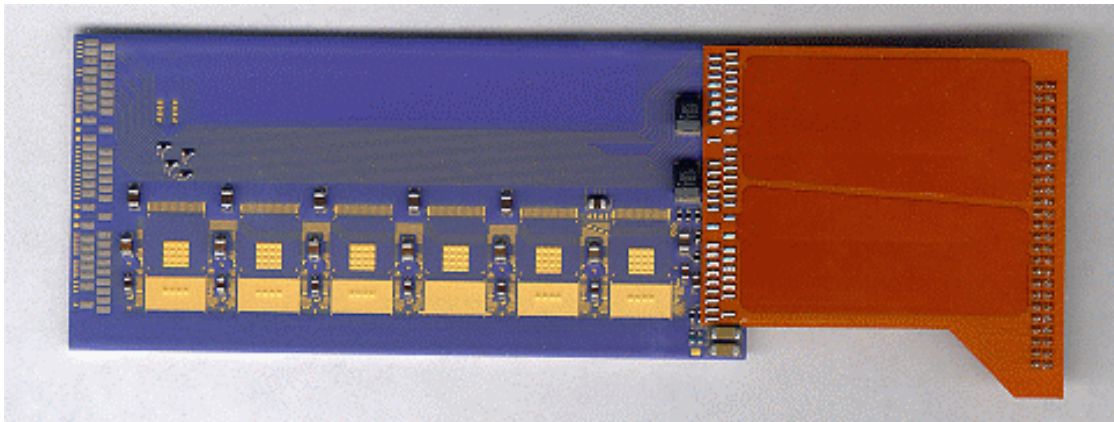


Silicon Strip Hybrids

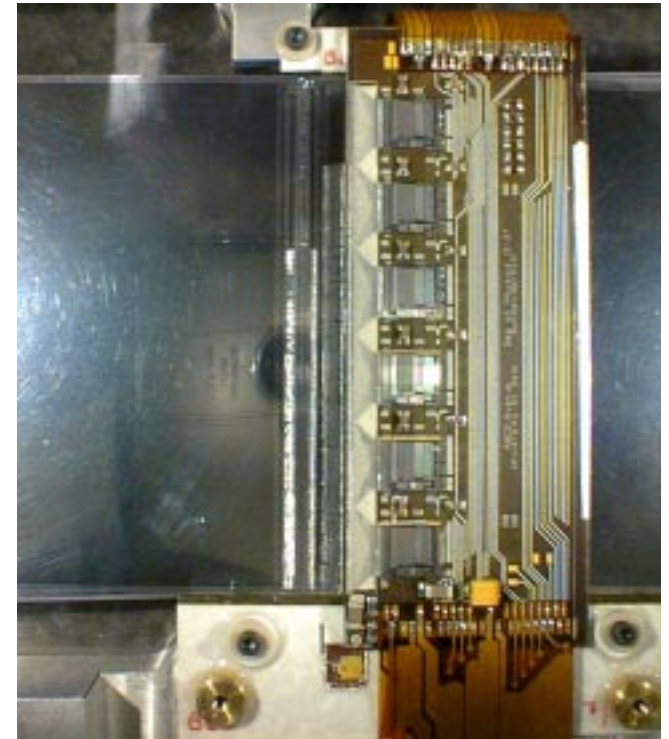
- Multiple technologies under consideration for hybrids to hold ICs, connect to detector and conduct heat to cooling channels.
- Choice hoped for by December this year.
- U.S. has concentrated on beryllia, the most conservative choice



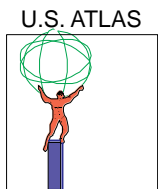
Copper on Kapton



Metal layers on beryllia

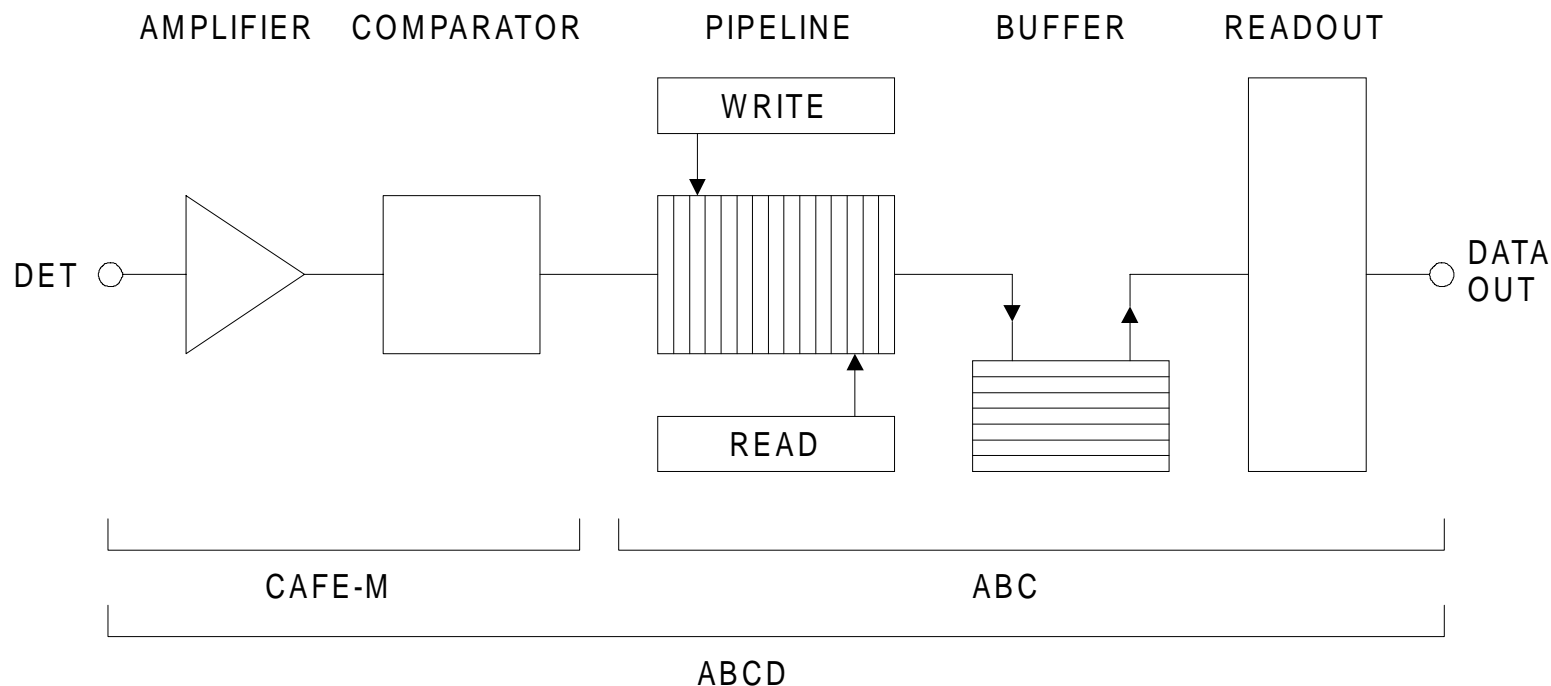


Metal layers/insulator
on pyrolytic graphite



Silicon Strip IC Electronics

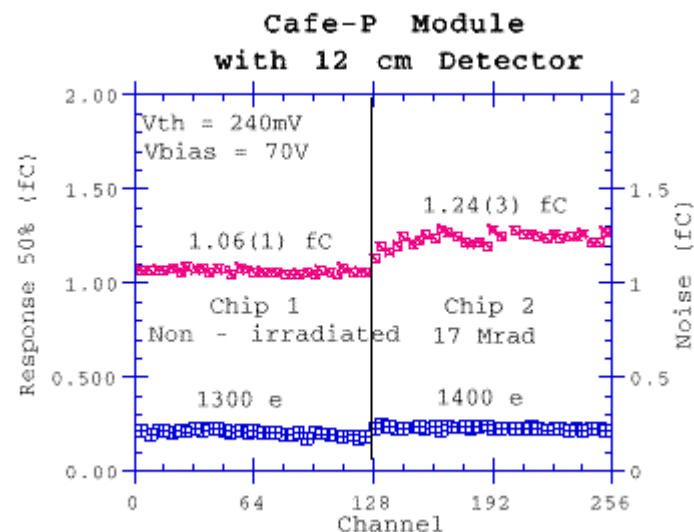
- Two rad-hard solutions under development - binary readout
 - ◆ CAFÉ(bipolar from Maxim) + ABC(CMOS from Honeywell) - 2 chips. This is the US cost baseline.
 - ◆ ABCD(BiCMOS from Temic) - 1 chip. Expected to be significantly cheaper than cost baseline.



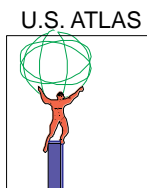


Silicon Strip IC Electronics

- First prototypes for all three ICs were not satisfactory.
- All have been redesigned (rather painfully and definitely slowly)
- We want to make a vendor choice by December to hold to U.S. baseline schedule.

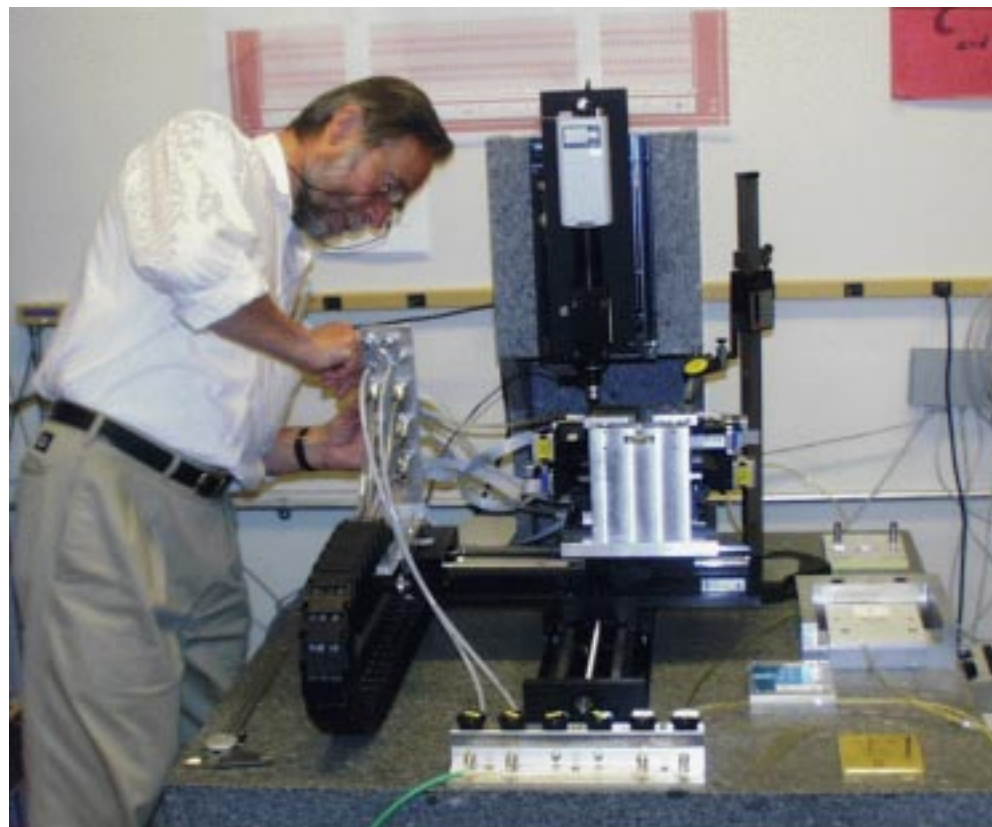
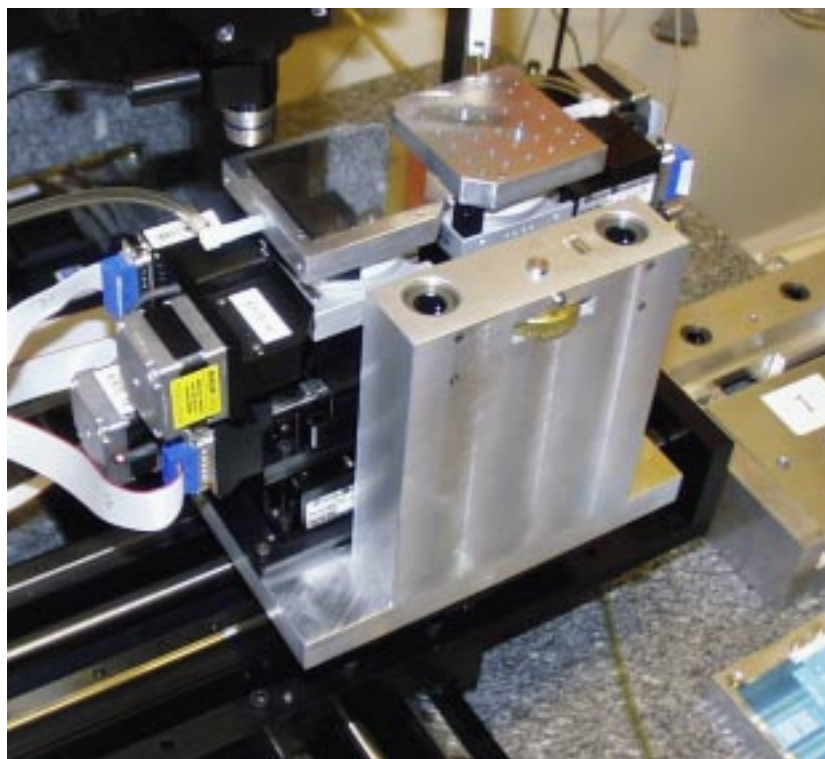


- CAFÉ-P returned April 8 and looks OK so far (see plot) but really need mating chip ABC to test fully
- ABC in fab and expect out by early August. One dumb bug discovered after starting fab but not fatal.
- ABCD returned July 7 and 2 wafers under test. Temic processing out of spec for this lot but items out of spec not believed to affect performance (but have to verify). Not good to make vendor selection based on out-of-spec lot, so negotiation underway with Temic to reprocess (for free). Test results on wafers so far look encouraging. Good enough that we want some of out-of-spec to get going earlier.



Silicon Strip Module Production

- 700 some modules(out of about 4000) to be made at LBNL and tested at Santa Cruz and LBNL
- First dummy modules fabricated.
- Few active modules fabricated or being fabricated(need ICs!)

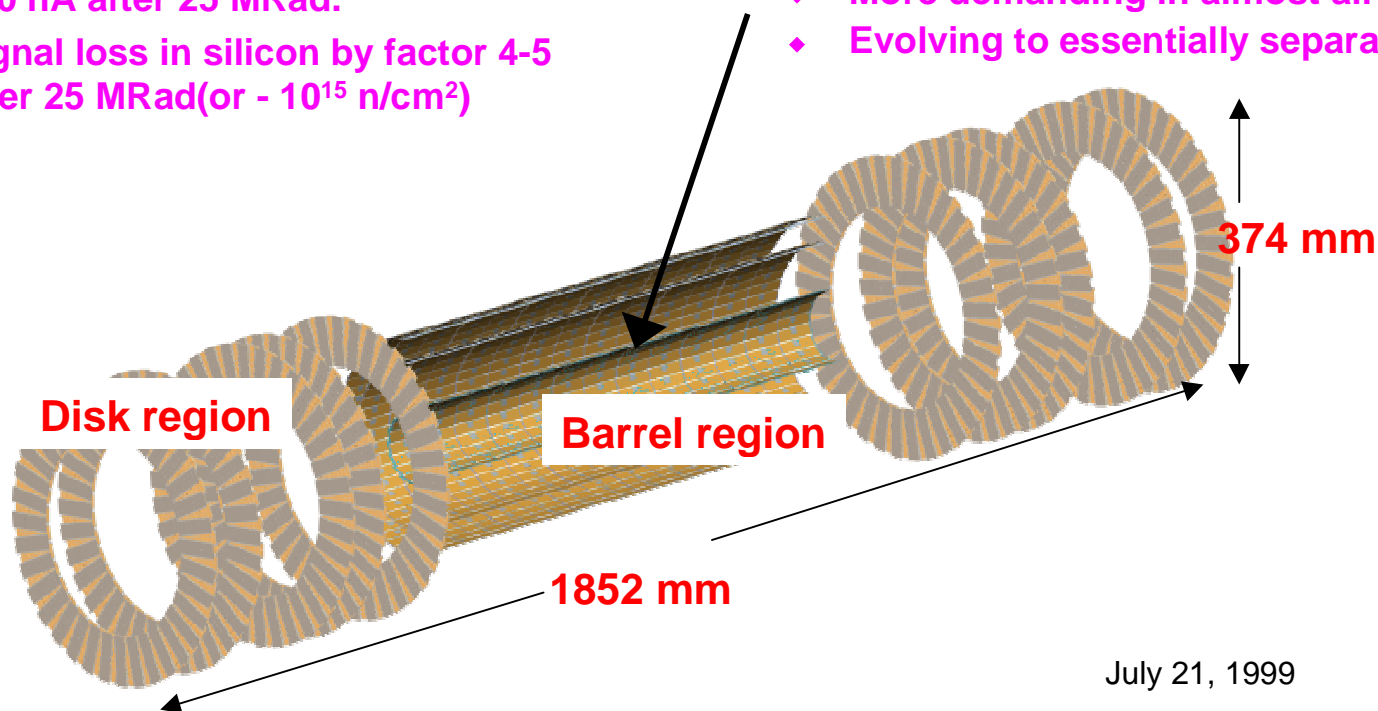


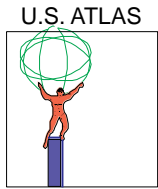
- Precision and computer controlled(more or less at the moment) tooling exists.
- Clean rooms under preparation to be ready by end of September.



Pixel System

- **Layout**
 - ◆ 3 barrel layers, 2 x 5 disk layers
 - ◆ Three space points for $|\eta| < 2.5$
 - ◆ Modular construction (about 2000 modules)
- **Radiation hardness**
 - ◆ Lifetime dose - 25 MRad at 10 cm
 - ◆ Leakage current in $50\mu\text{x}300\mu$ pixel is - 30 nA after 25 MRad.
 - ◆ Signal loss in silicon by factor 4-5 after 25 MRad (or - 10^{15} n/cm²)
- **Pattern recognition**
 - ◆ Space points. Occupancy of - 10^{-4}
- **Performance**
 - ◆ Critical for b tagging (big physics impact)
 - ◆ Need for 3 hits confirmed by simulation
- **Trigger**
 - ◆ Space points -> L2 trigger
- **B-Layer**
 - ◆ More demanding in almost all aspects
 - ◆ Evolving to essentially separate project





Pixel Institutions - Small Group

- Canada

- ◆ University of Toronto

- Czech Republic

- ◆ Academy of Sciences - Institute of Physics of Prague, Charles University of Prague, Czech Technical University of Prague

- France

- ◆ CPPM, Marseille

- Germany

- ◆ Bonn University, Dortmund University, Siegen University, Bergische University - Wuppertal

- Italy

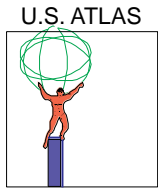
- ◆ INFN and University of Genova, INFN and University of Milano, INFN and University of Udine

- Netherlands

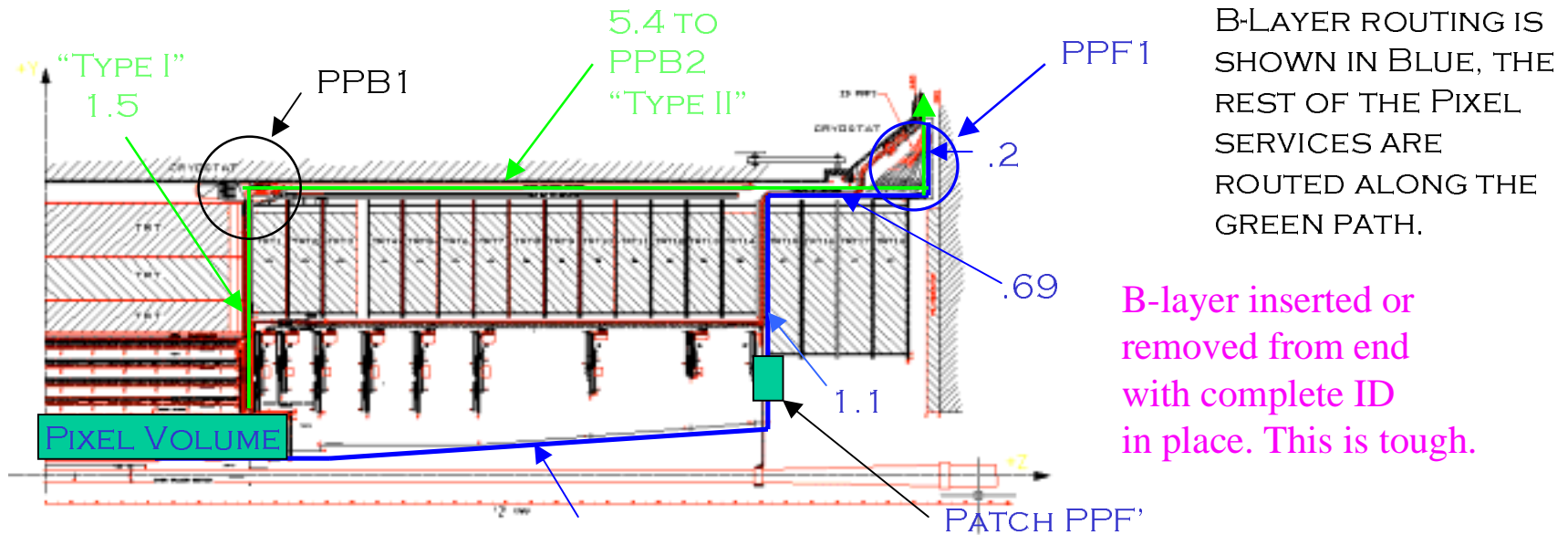
- ◆ NIKHEF - Amsterdam

- USA

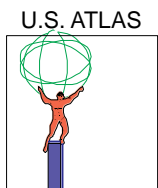
- ◆ University of New York - Albany, LBL and University of California - Berkeley, University of California - Irvine, University of New Mexico - Albuquerque, University of Oklahoma, University of California - Santa Cruz, University of Wisconsin - Madison



Pixel Layout and General Features



- The pixel layout has slowly evolved in the last years. Area reduced in disk region to fit completely within barrel region, detailed changes as module design has matured.
- Detailed comparison made of track efficiencies and impact on performance of 2 vs 3 pixel layers. Conclusion need 3 layers/hits - confusion significantly worse with only B-layer and one other hit. Need full pixel system for both good tracking and B-layer critical for b-tagging.

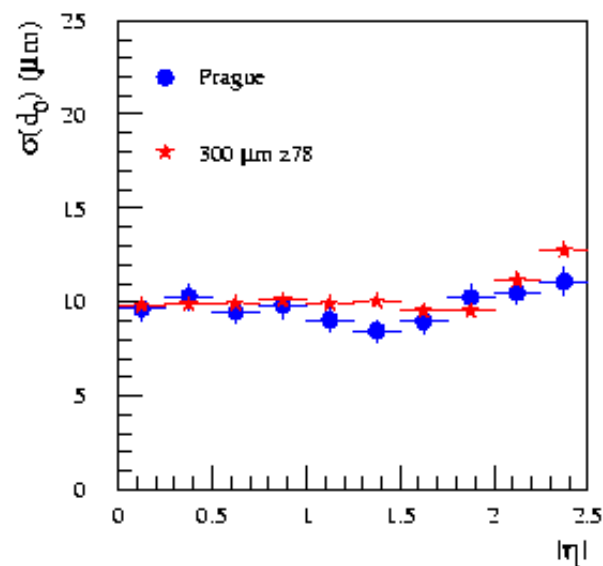


Pixel Size Studies

- Most recently, have studied 50x400 micron pixels vs baseline of 50x300 micron. Why? DMILL electronics not dense enough to go below 400 micron pixel length. Also reduces power. Preliminary conclusion is that 400 is OK except in B-layer and formal ECR in process to make this change. Implication is different electronics (eg. Honeywell) for B-layer required.

IP resolutions for Prague vs Z78 layout

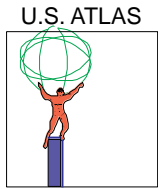
Transverse IP resolution. Z78 layout with 300 μm flex modules. Prague layout 315 μm MCMD in B-layer, 400 μm flex in outer layers.





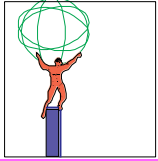
Pixel Development Strategy

- This is a new technology but one that is required for ATLAS because of the radiation levels and track density. Staging is very risky. Repair only if major failure. All implies get it right.
- Development strategy is simple - prototype everything, usually in multiple stages, before reaching production status
 - ◆ **Sensors**
 - ▲ Round 1 complete
 - ▲ Round 1b complete
 - ▲ Round 2 started fab
 - ◆ **Electronics**
 - ▲ Rad-soft complete(but used for module development)
 - ▲ 1st rad-hard design(DMILL) almost complete. With Honeywell later. US plan is for 2nd round of prototype after vendor selection.
 - ◆ **Hybrids**
 - ▲ Round 1 complete
 - ▲ Round 1.1 and 1.2(two different vendors) in fab or just completed
 - ▲ Round 2 started design
 - ▲ Round 3 planned
 - ◆ **Modules**
 - ▲ Round 1 complete
 - ▲ Round 1.x started
 - ▲ Round 2 and 3 planned
 - ◆ **Mechanics**
 - ▲ Round 1 started
 - ▲ Round 2 planned for some, but not all parts



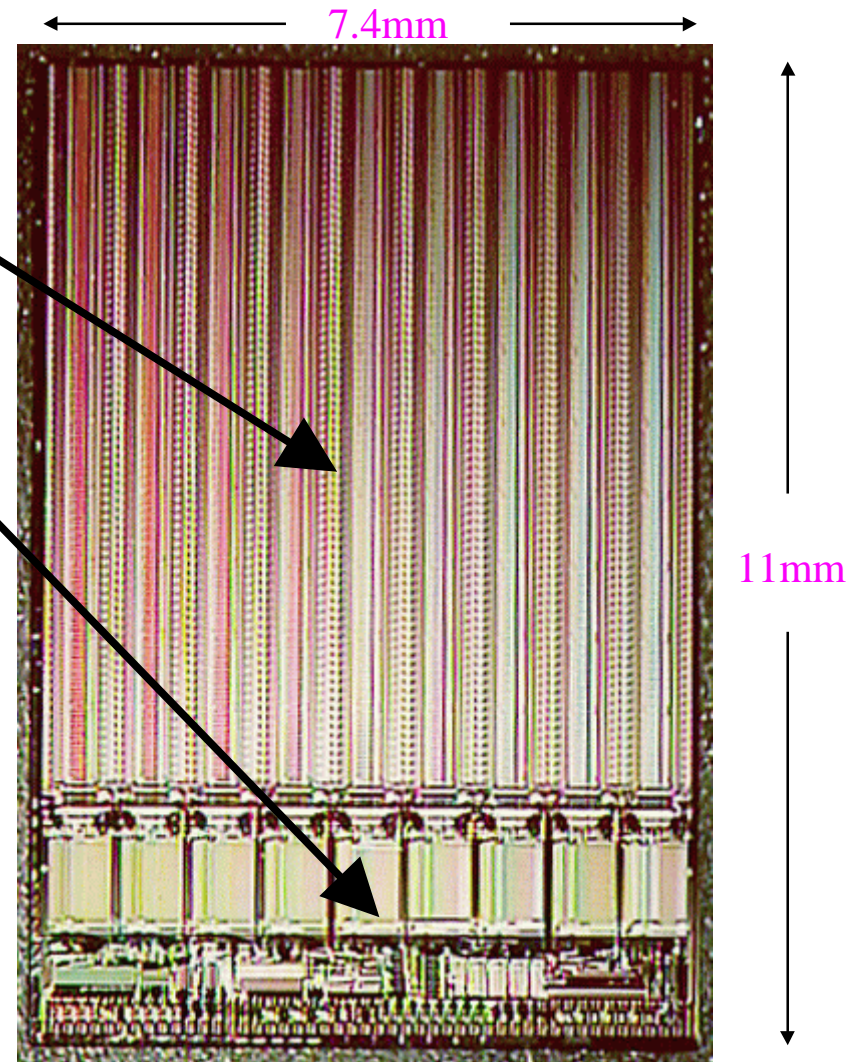
Pixel Sensors

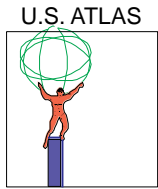
- **Critical requirements**
 - ◆ Useful signal up to fluences of 10^{15} n/cm²
 - ▲ Must be able to operate partially depleted => n implants in n-substrate
 - ▲ Maximum voltage feasible(600 V we hope)
 - ◆ High efficiency. Optimize implant geometry to obtain uniform as possible charge collection.
 - ◆ Capability to test. How to ground pixels? Clever scheme invented.
- **Important requirements**
 - ◆ Minimize cross talk(with electronics)
 - ◆ Minimize capacitance(=> noise)
- These essential requirements have been met by recent prototypes
- B-layer requirements are more demanding unless replaced periodically (perhaps once per year at design luminosity) => alternative sensors with longer lifetime, if possible
 - ◆ oxygenated-silicon(this is part of 2nd prototype round under fab)?
 - ◆ Diamond?
 - ◆ will have data by next summer to evaluate feasibility of reaching higher doses(100 Mrad?) including other components(electronics,)



Pixel Electronics

- **General features**
 - ◆ Active matrix 18x160 pixels
 - ◆ Inactive area for buffer and control
- **Critical requirements**
 - ◆ Time walk <20 ns
 - ◆ Timing uniformity across array(<few ns)
 - ◆ Low threshold(2-3K e⁻s)
 - ◆ Threshold uniformity (implemented by having DAC in each pixel)
 - ◆ Low noise(<few hundred e⁻)
 - ◆ Low deadtime(<1% or so)
 - ◆ Robust(dead pixel OK, dead column not good, dead chip bad)
 - ◆ All of the above at 25 Mrad or more
- **Important requirements**
 - ◆ Time-Over-Threshold(TOT) measurement of charge
 - ◆ Maximize active area
 - ◆ Die size with acceptable yield
 - ◆ Thin(150 micron goal)

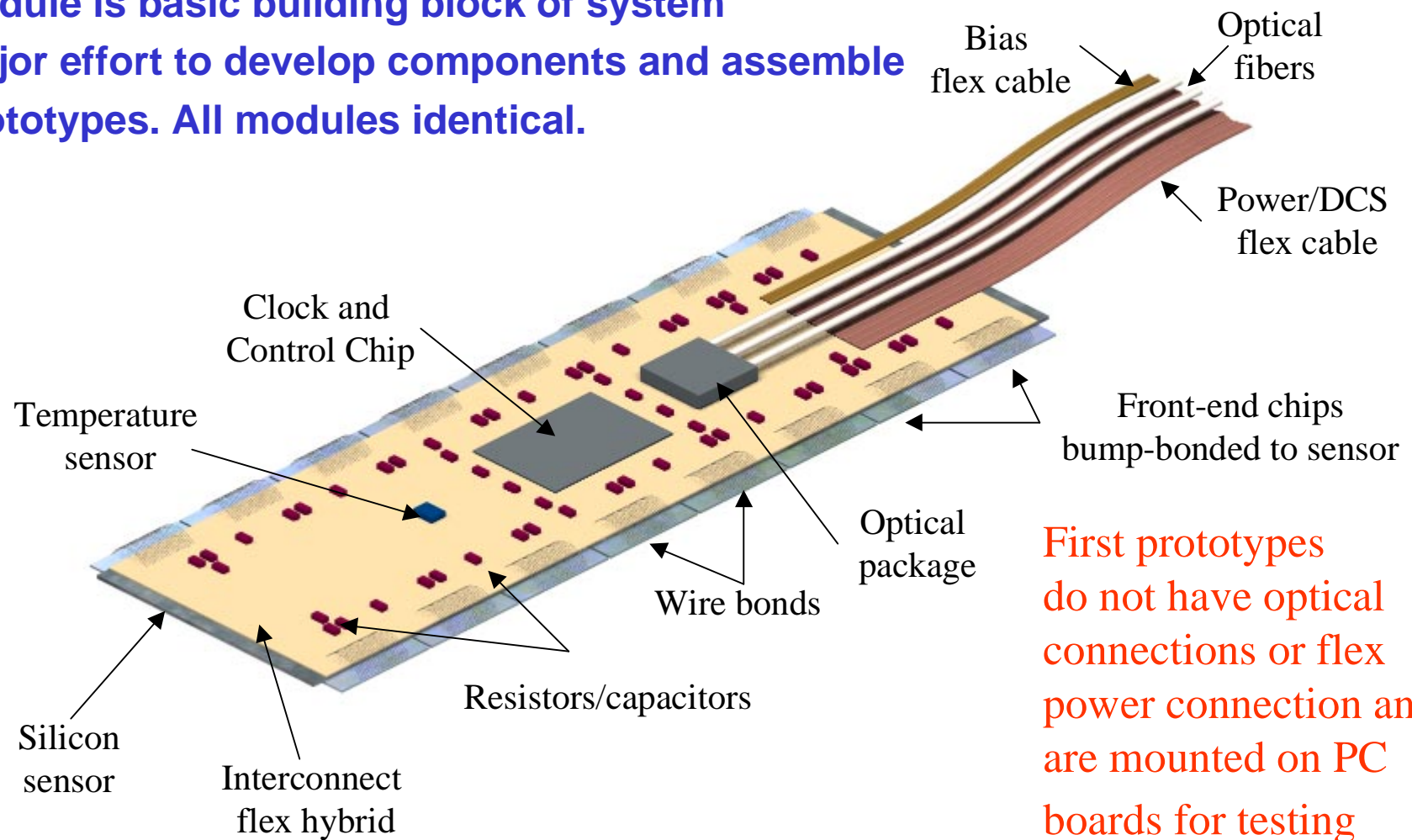




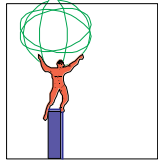
Pixel Module

Module is basic building block of system

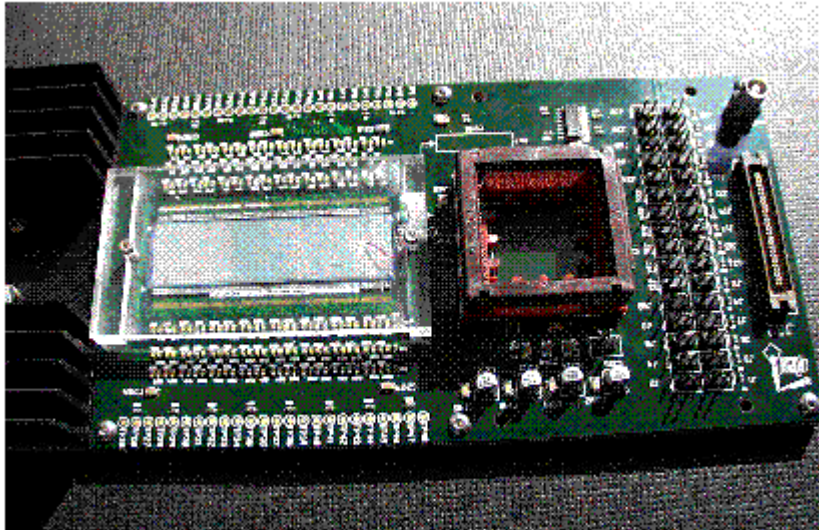
Major effort to develop components and assemble prototypes. All modules identical.



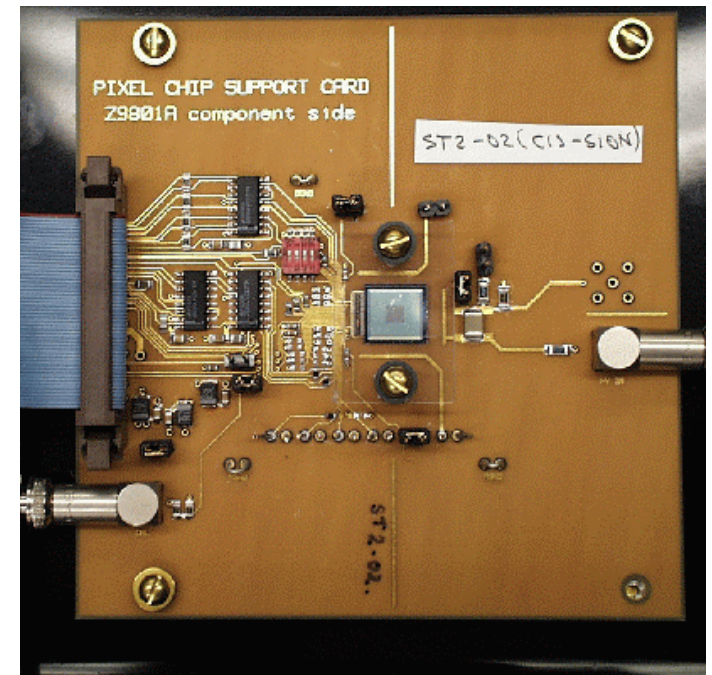
First prototypes do not have optical connections or flex power connection and are mounted on PC boards for testing



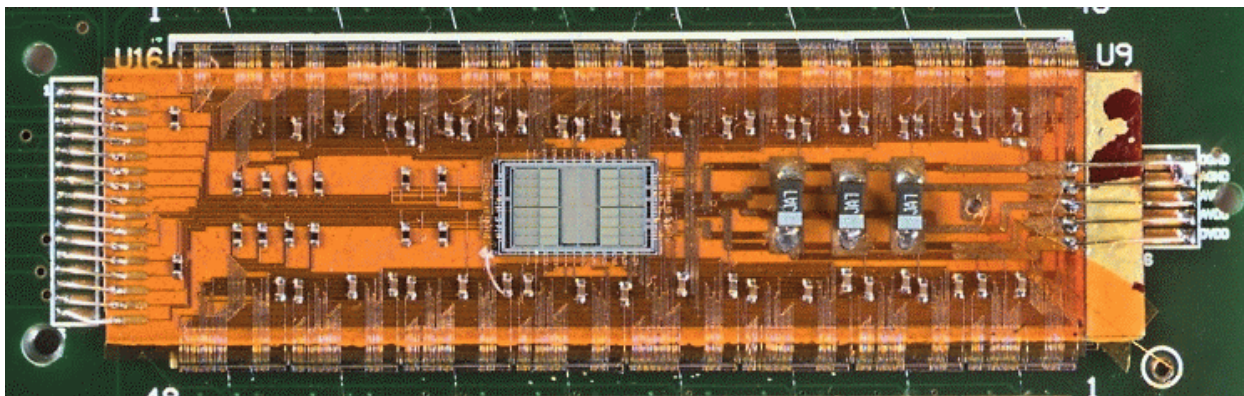
What Has Been Tested



Bare 16-chip modules



Dozens of single
chip/sensor assemblies
of different types



16-chip modules with flex hybrid



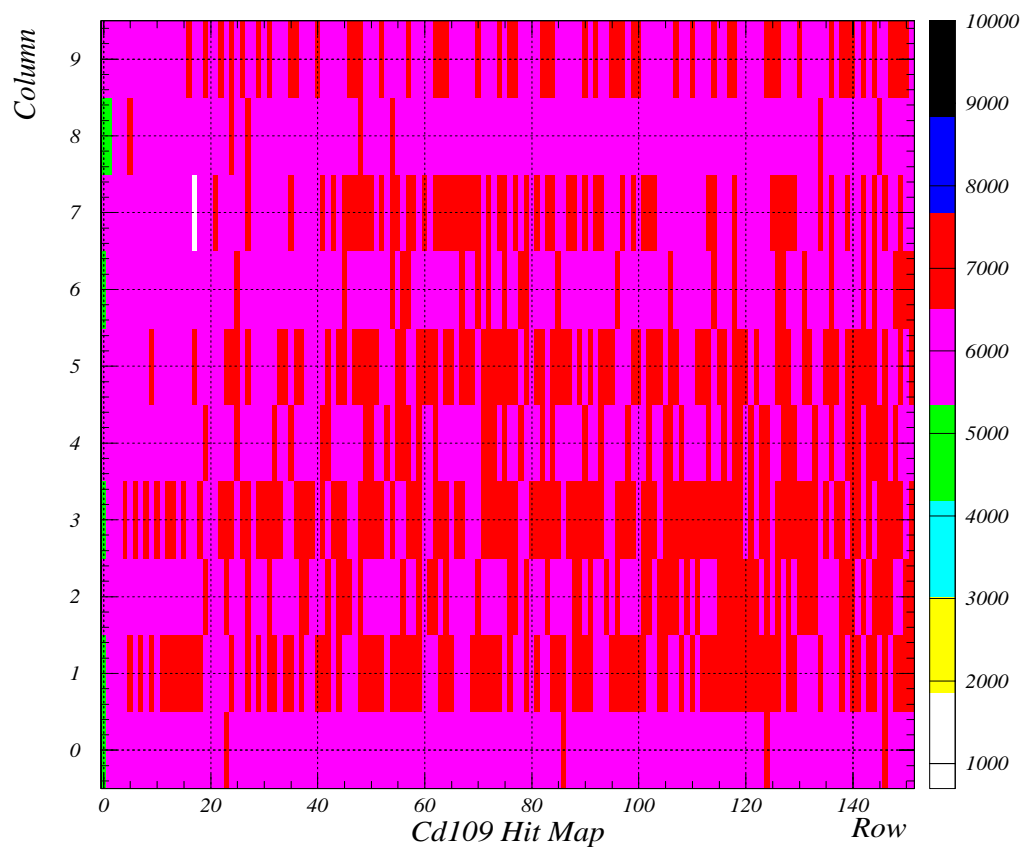
Lab and Test Beam Results - Summary

- Extensive lab tests, three test beam runs in 1998, one in 1999 and two more to go in 1999. Very successful(so far).
- Highlights
 - ◆ Only rad-soft ICs so far(3 variants used - FE - A, - B, - C)
 - ◆ Dozens of single-chip/detectors have been operated successfully with multiple detector types and front-end ICs
 - ◆ 16 chip modules have been operated successfully
 - ◆ Detectors irradiated to lifetime fluence expected at LHC(10^{15}) have been read-out in a test beam with efficiency near 100%
 - ◆ Operation below full depletion voltage demonstrated
 - ◆ Preferred detector type identified in these studies
 - ◆ Timing performance needed to identify bunch crossings has been demonstrated, albeit not at full system level.
 - ◆ Operation at thresholds 2,000-3,000 electrons demonstrated
 - ◆ Threshold uniformity demonstrated.
 - ◆ Spatial resolution as expected
- Conclusion
 - ◆ Proof-of-principle of pixel concept successful



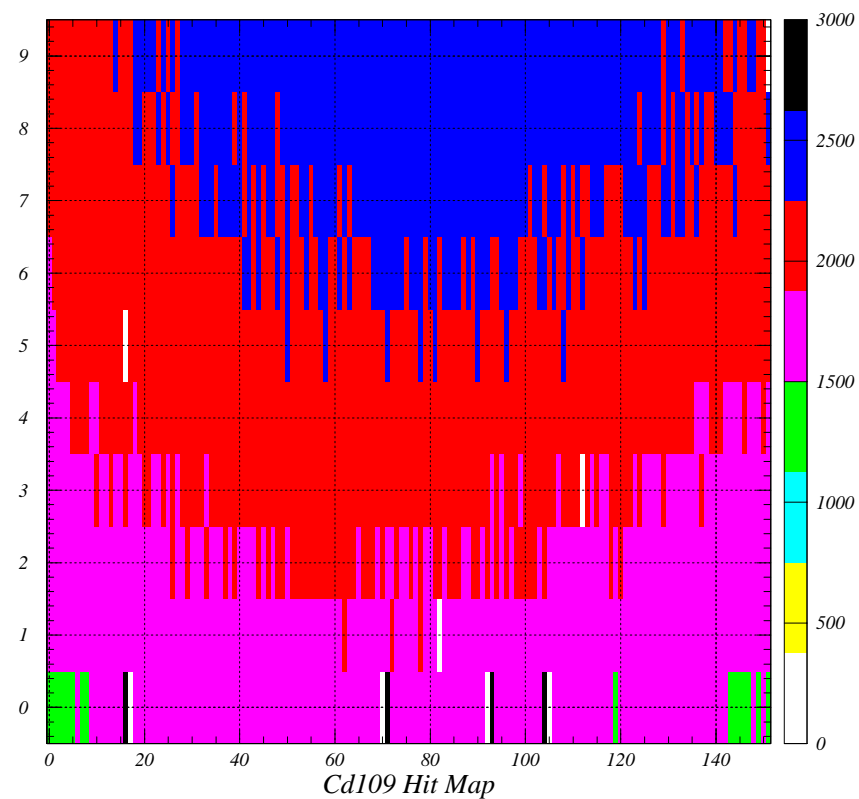
Photon Source Test of FE-B and Detectors

CIS_01 single-metal ST2_03 Cd109

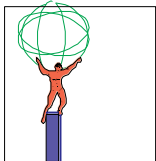


21

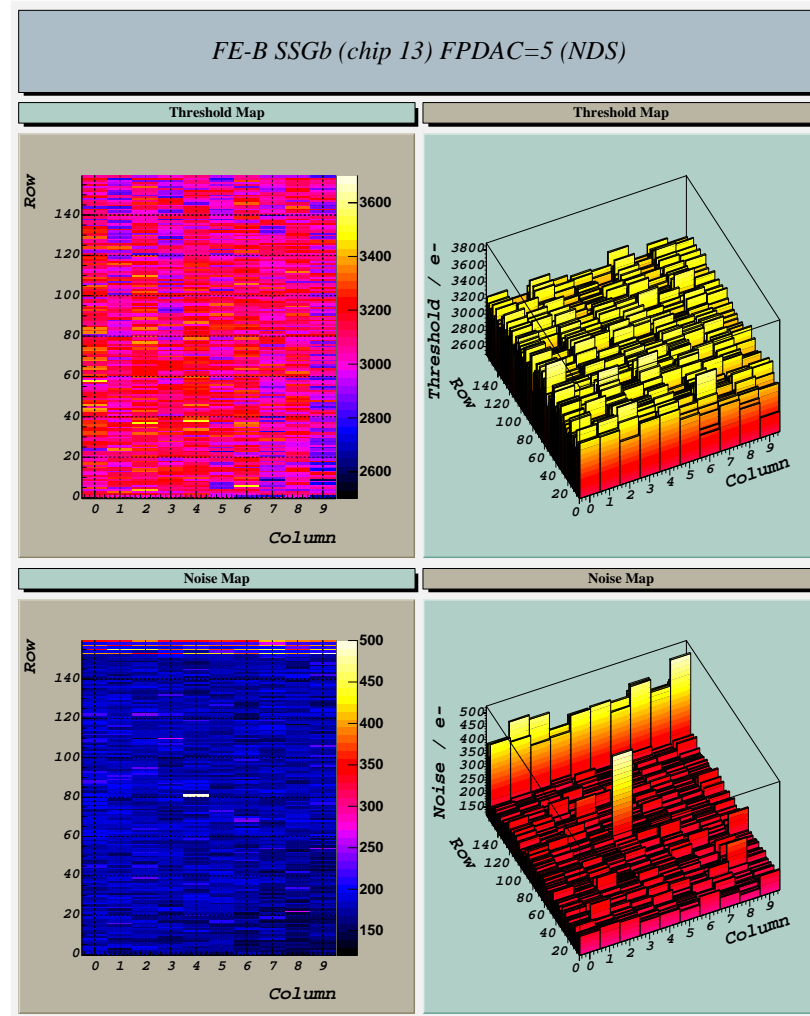
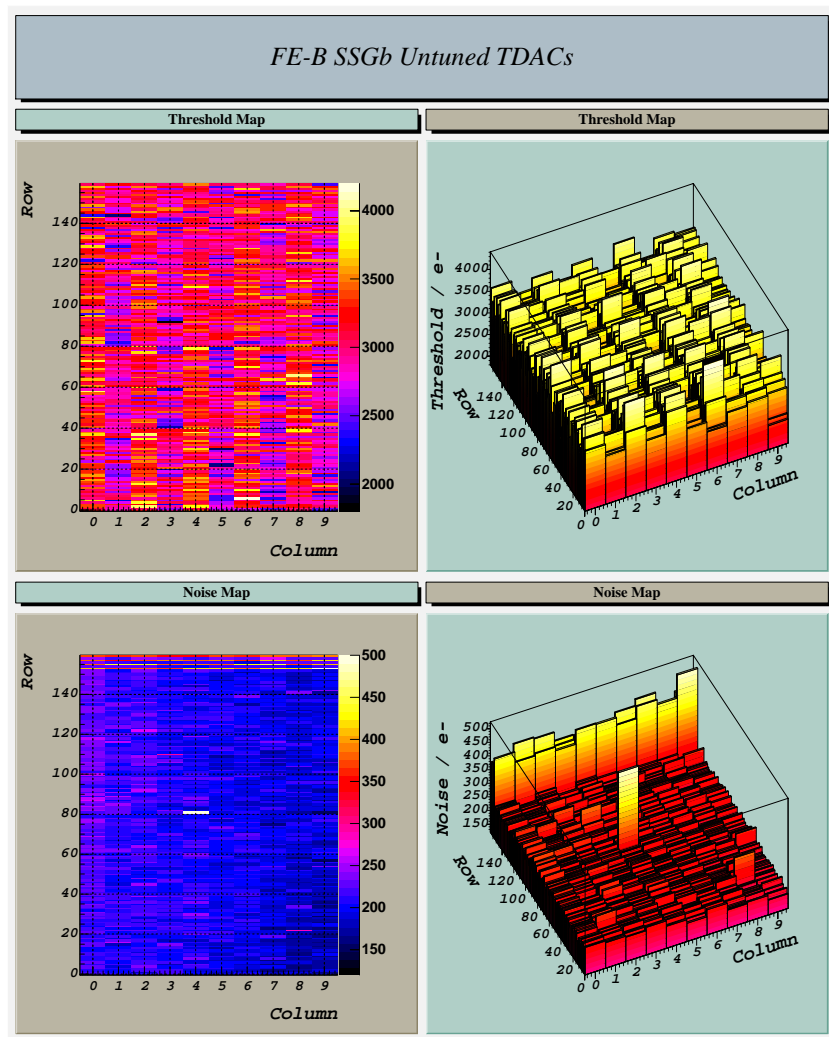
CIS ST1 Cd109

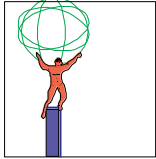


July 21, 1999

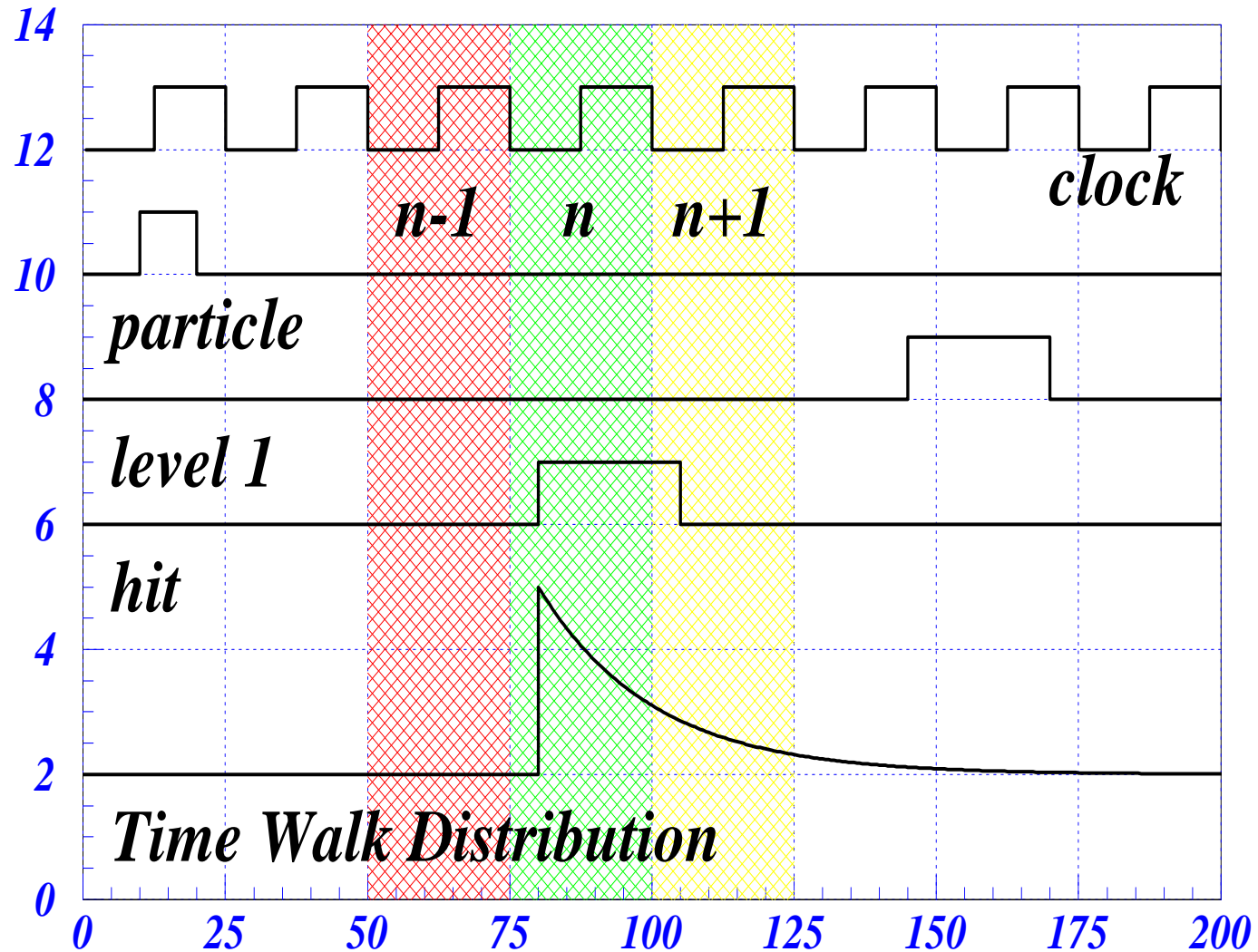


Threshold Tuning and Noise





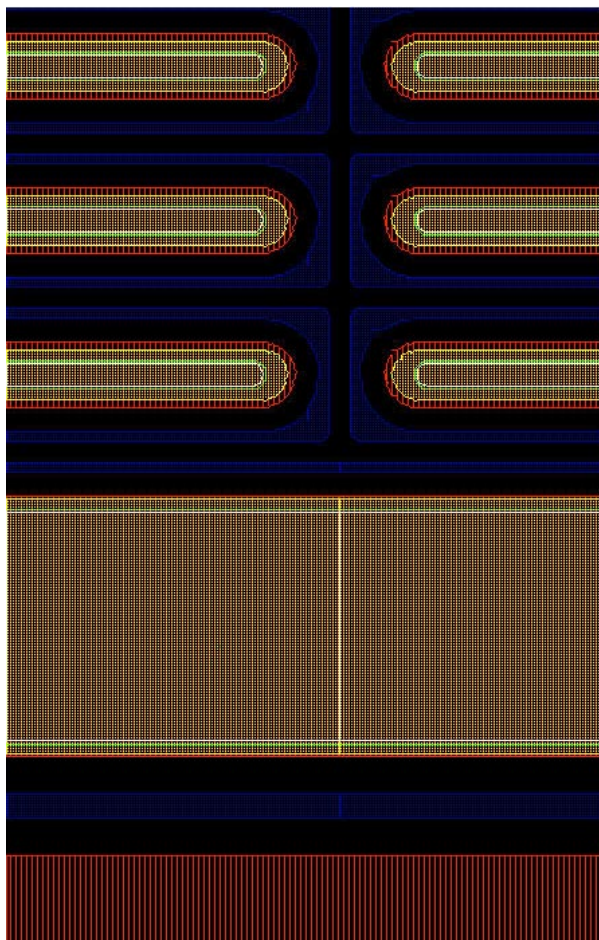
Efficiency and Timing in Test Beam



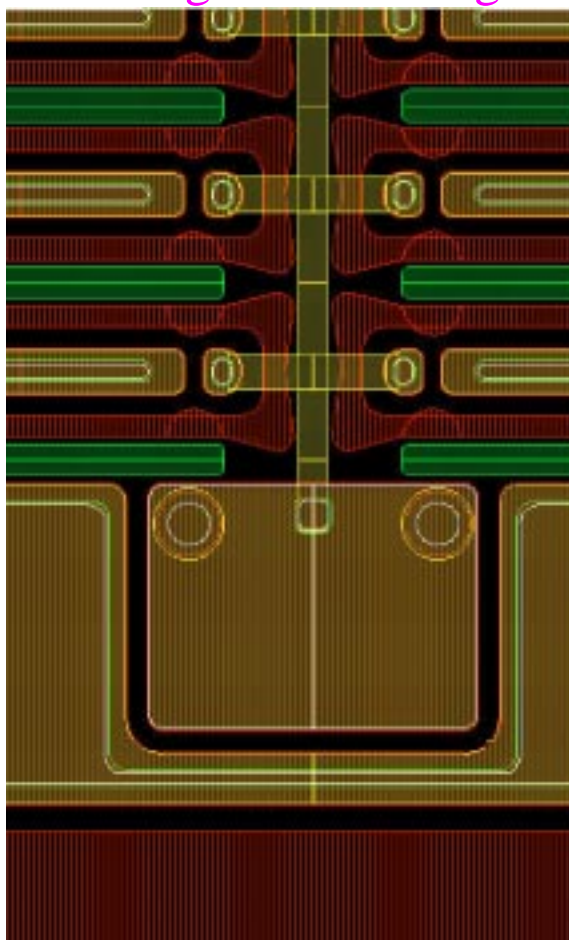


Summary of Detector Layouts

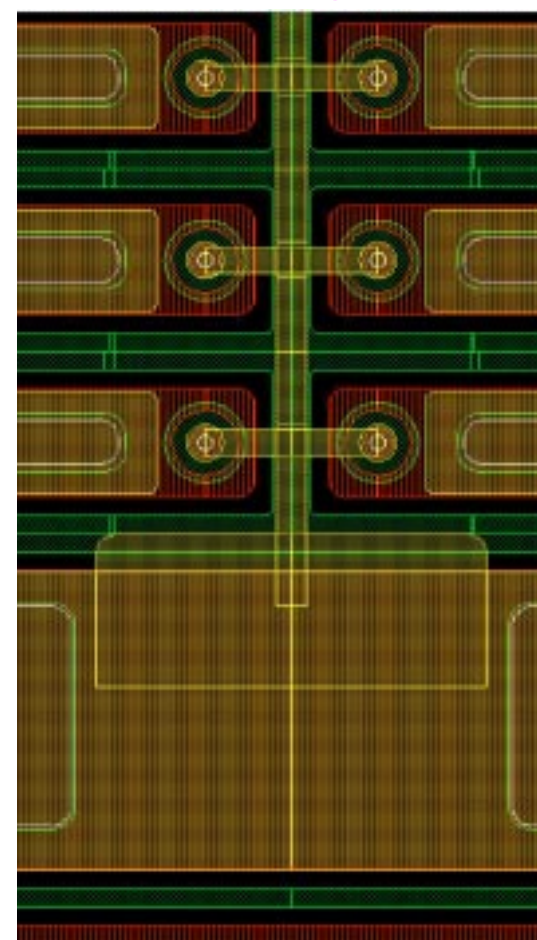
Tile 1 - p-stop isolation

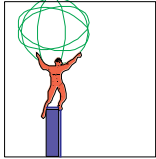


Tile 2 - p-spray isolation
bias grid for testing



Tile 2 modified
bias grid



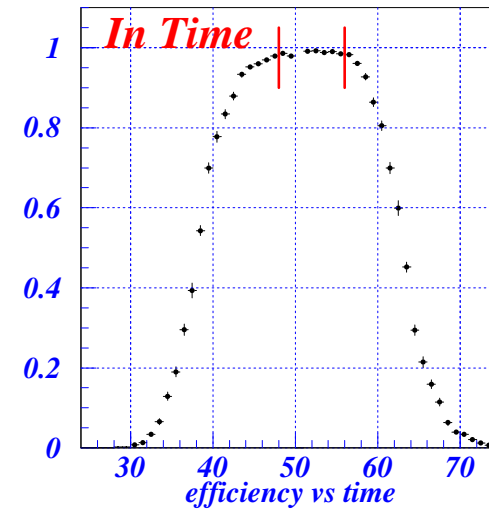


In-Time Efficiencies

Detector Tile 2 v1.0 - not Irradiated - Thr. 3 Ke

Efficiency 98.8% **Losses 1.2%**

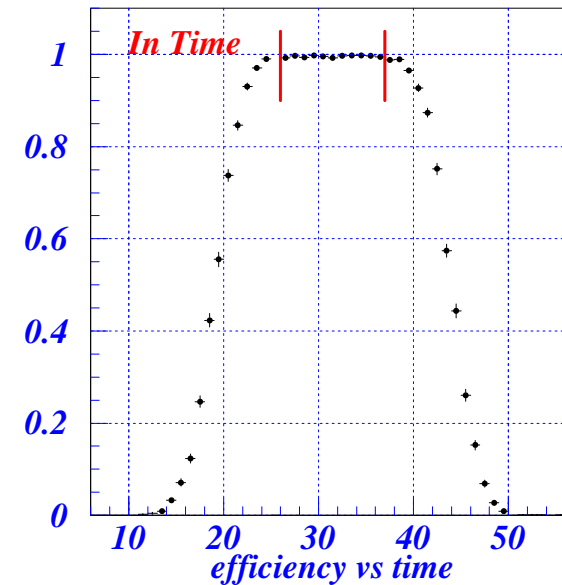
1 hit	82.0	0 hits	0.4
2 hits	14.6	not matched	0.2
>2 hits	2.2	not in time	0.6

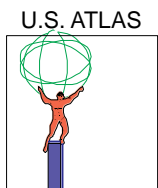


Detector Tile 1 v1.0 - not Irradiated - Thr. 3 Ke

Efficiency 99.6% **Losses 0.4**

1 hit	72.0	0 hits	0.1
2 hits	25.2	not matched	0.2
>2 hits	2.4	not in time	0.1



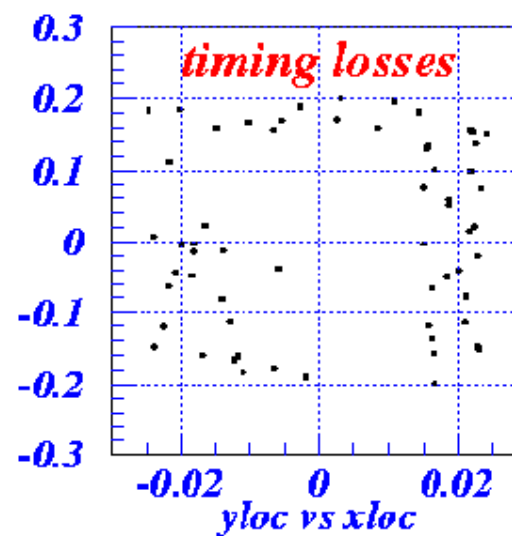
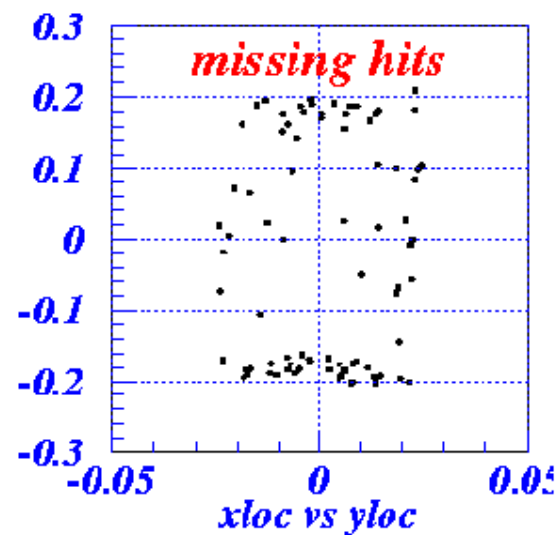
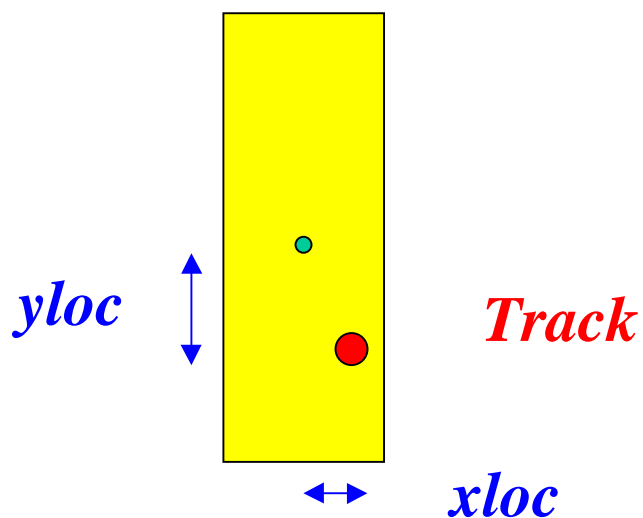


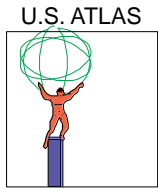
Irradiated Detectors

Tile 2 - Irradiated $V_{\text{bias}} = 600 \text{ V}$

Fluence 10^{15} n/cm^2 - **Thr.** 3 Ke

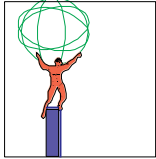
Efficiency	95.3%	Losses	4.7%
1 hit	86.3	0 hits	2.2
2 hits	7.6	not matched	0.1
>2 hits	1.4	not in time	2.4





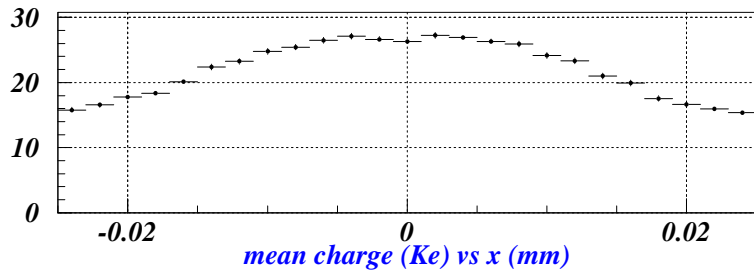
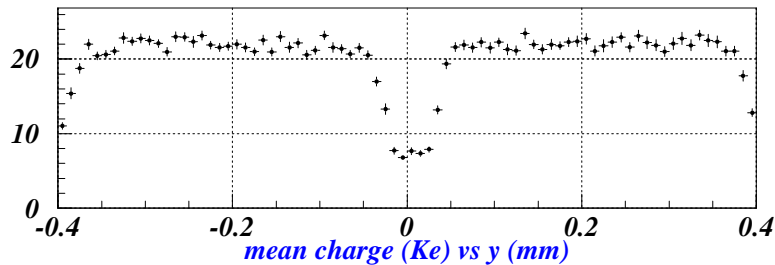
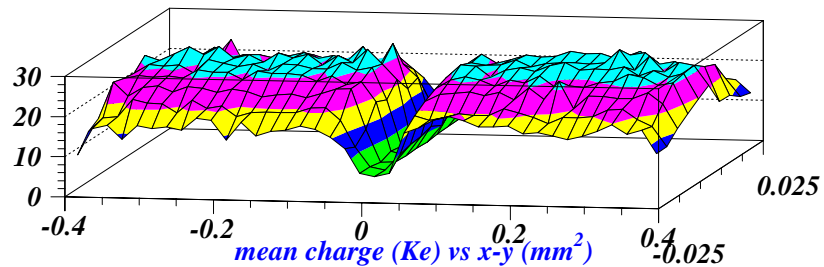
Implications of Results

- **Tile 1 design has good efficiency and uniformity before irradiation but after irradiation, cannot increase bias voltage beyond about 100-150 volts - too low. And does not have bias grid for testing.**
- **Tile 2 design has OK efficiency, non-uniform response but has worked up to 600 volts after irradiation and has bias grid for testing => modify design to fix up.**
- **This was done in round 1b and tested a few months ago.**

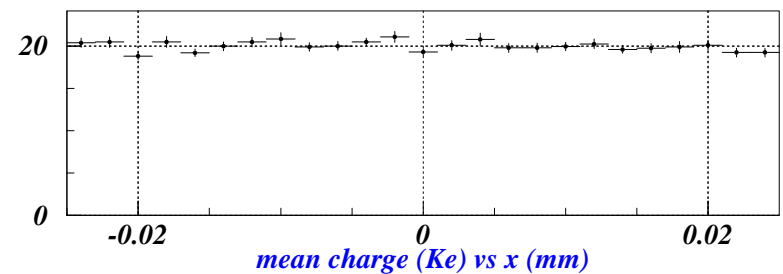
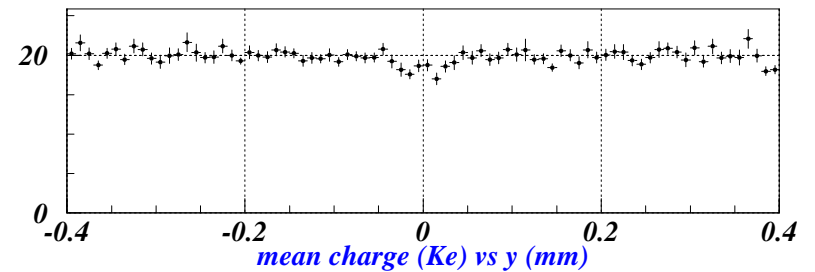
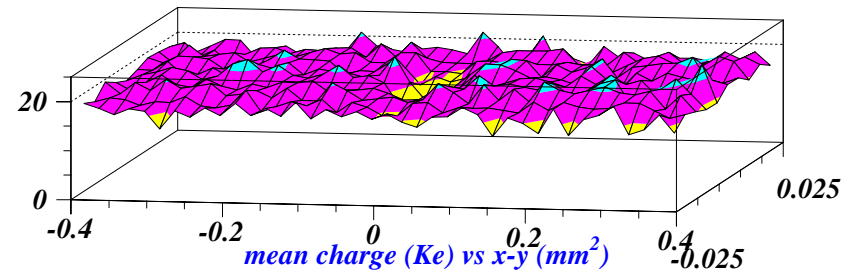


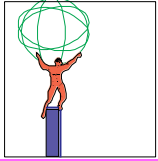
Charge Collection - PreRad

Tile 2 v1.0



Tile 2 v1b

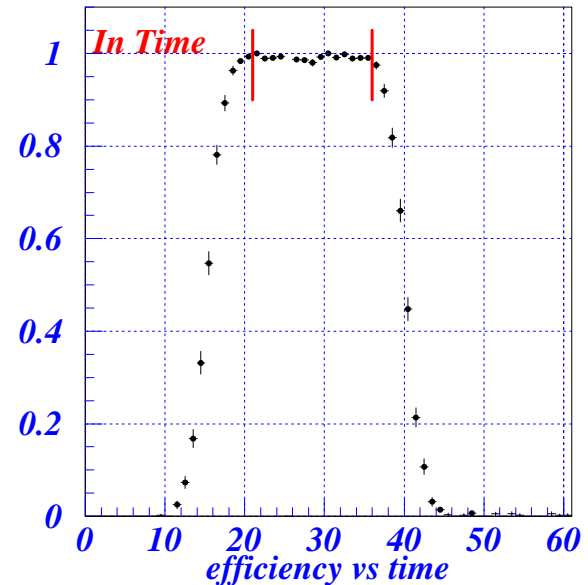




New Tile 2 Design Efficiency

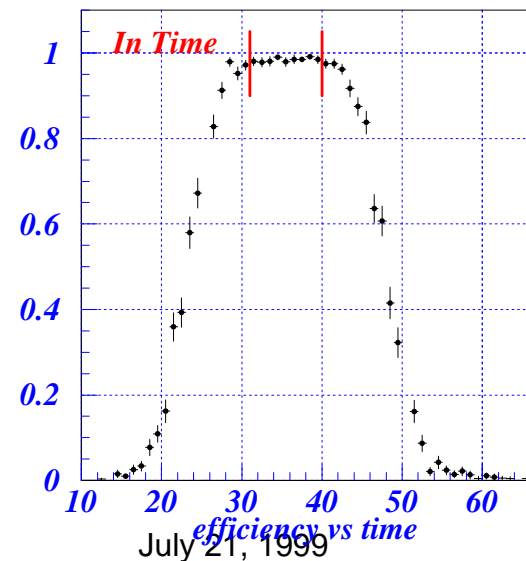
Detector Tile 2 new design (with bias grid) Not Irradiated - Thr. 3 Ke

Efficiency	99.1%	Losses	0.9%
1 hit	81.8	0 hits	0.4
2 hits	15.6	not matched	0.1
>2 hits	1.7	not in time	0.4



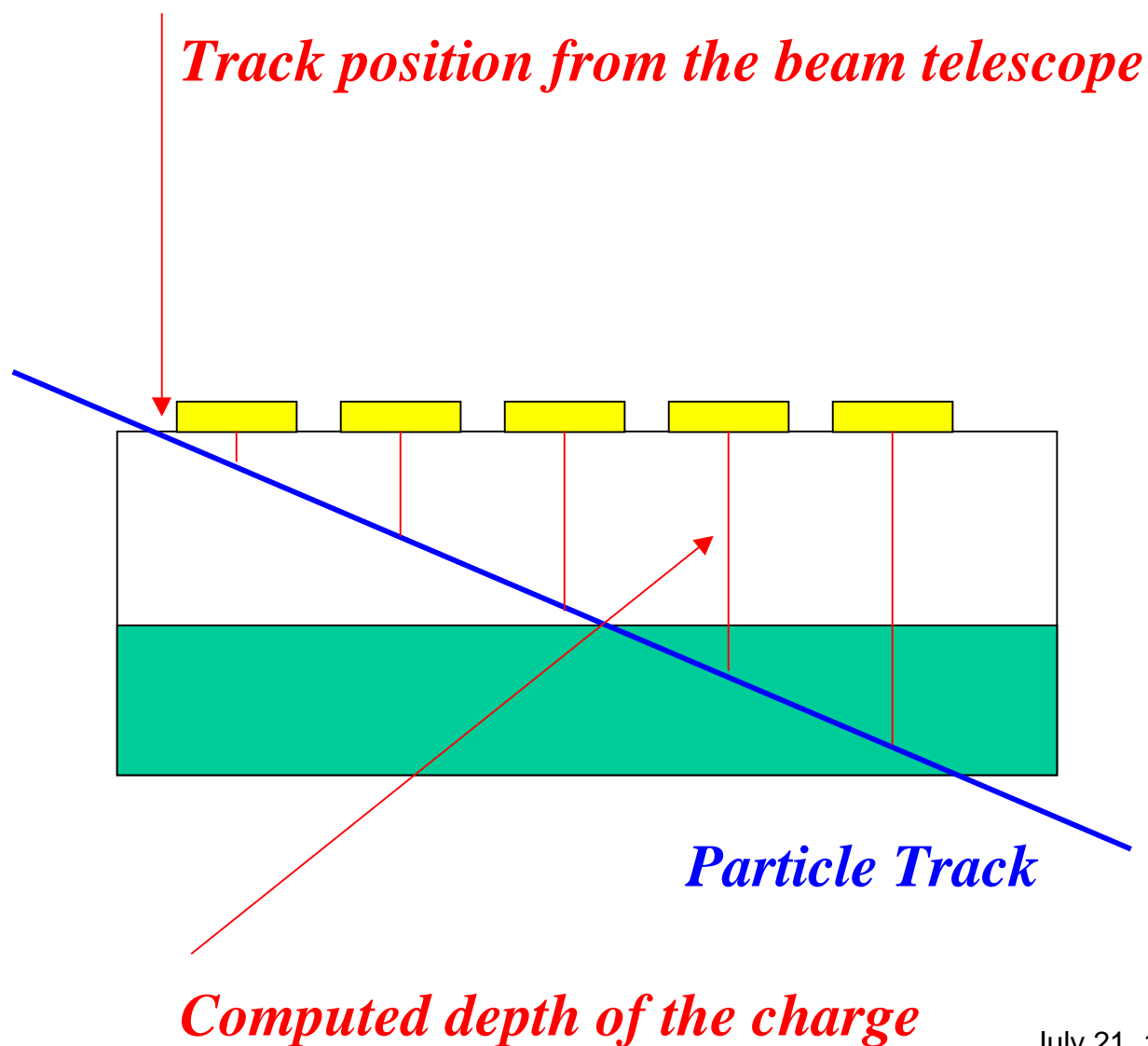
Detector Tile 2 - Irradiated $V_{\text{bias}} = 600 \text{ V}$ Fluence 10^{15} n/cm^2 - Thr. 3 Ke

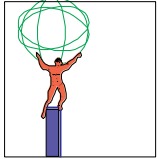
Efficiency	98.4%	Losses	1.6%
1 hit	94.2	0 hits	0.4
2 hits	3.1	not matched	0.0
>2 hits	1.1	not in time	1.2





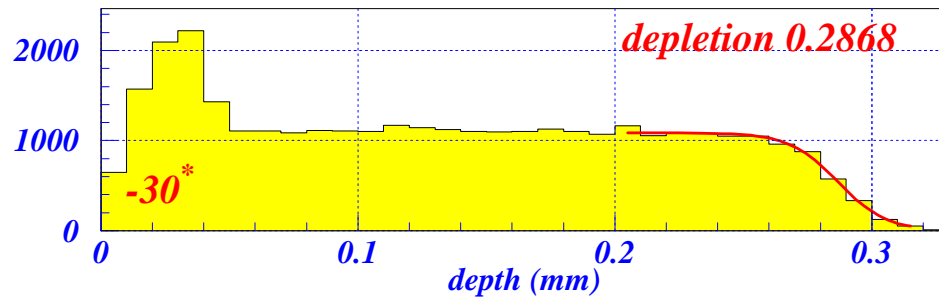
Depletion Depth Measurements



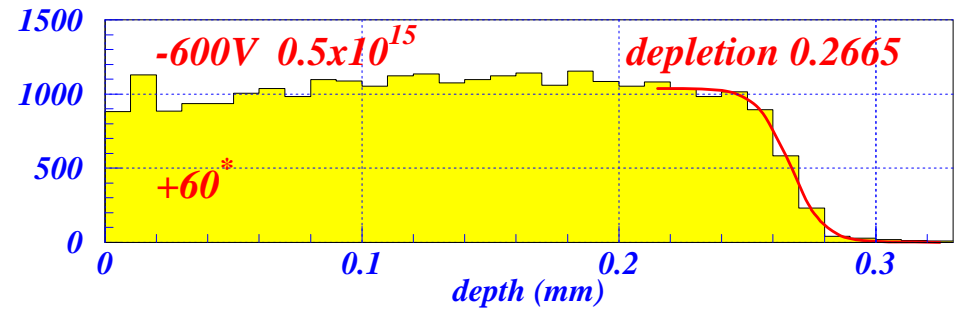
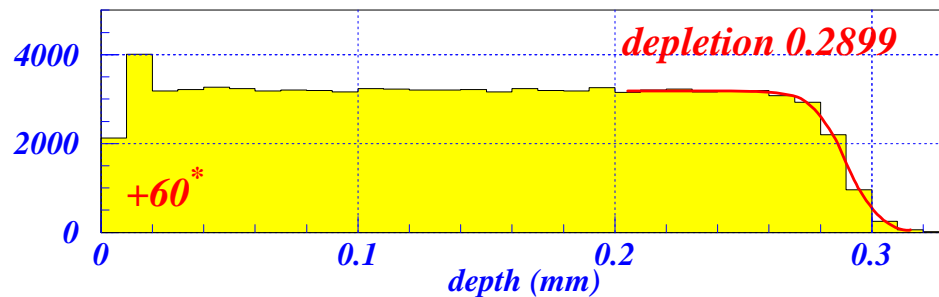
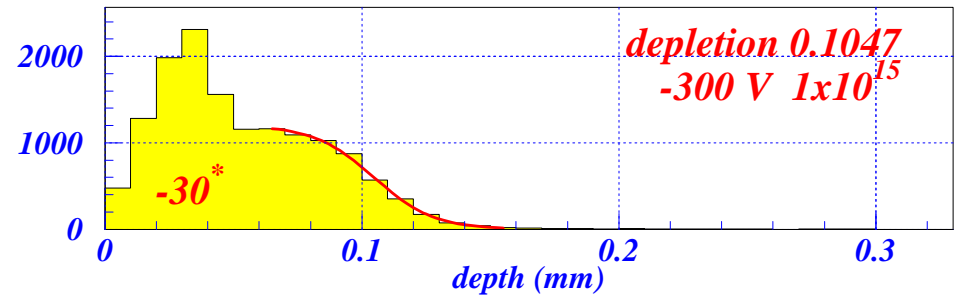
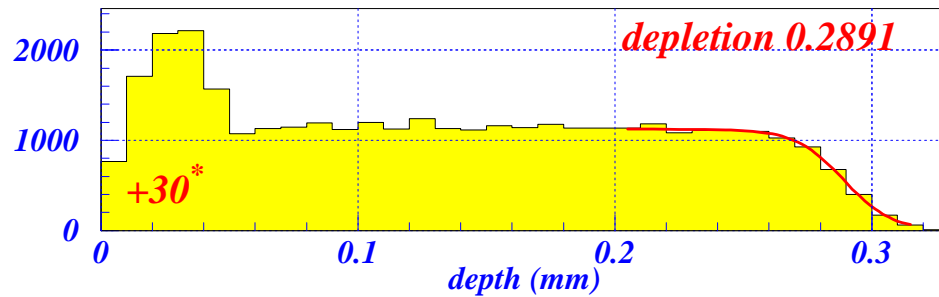
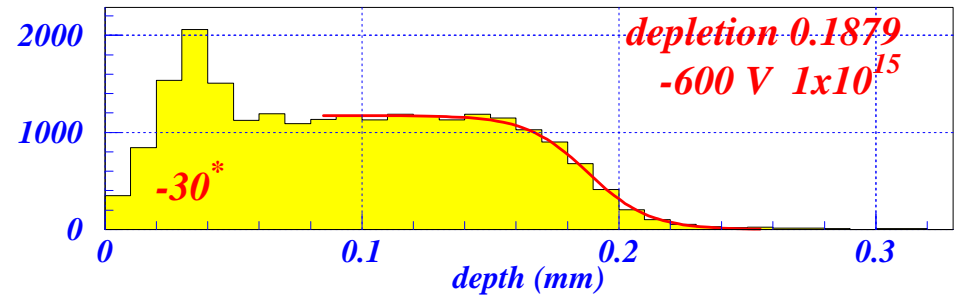


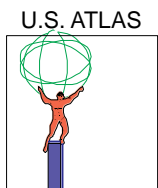
Depletion Depth Measurements

Not irradiated - depletion depth

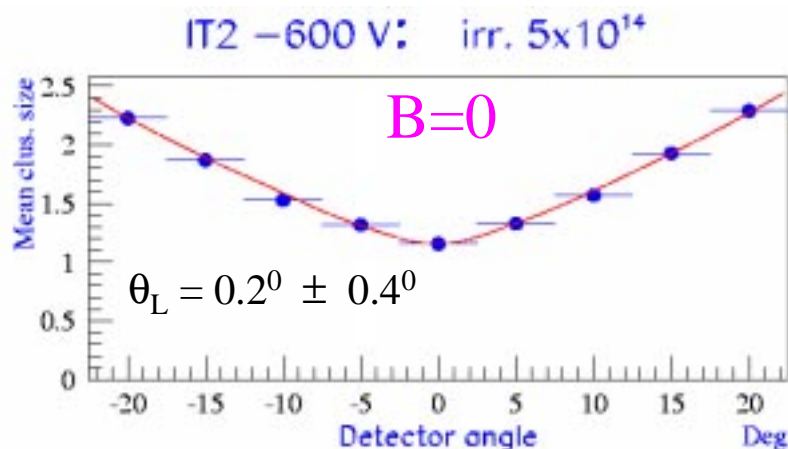


Irradiated - depletion depth



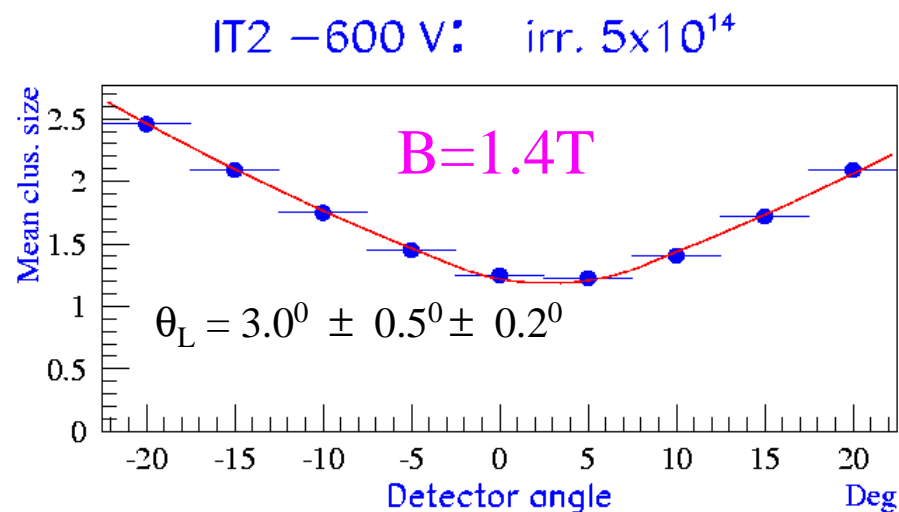
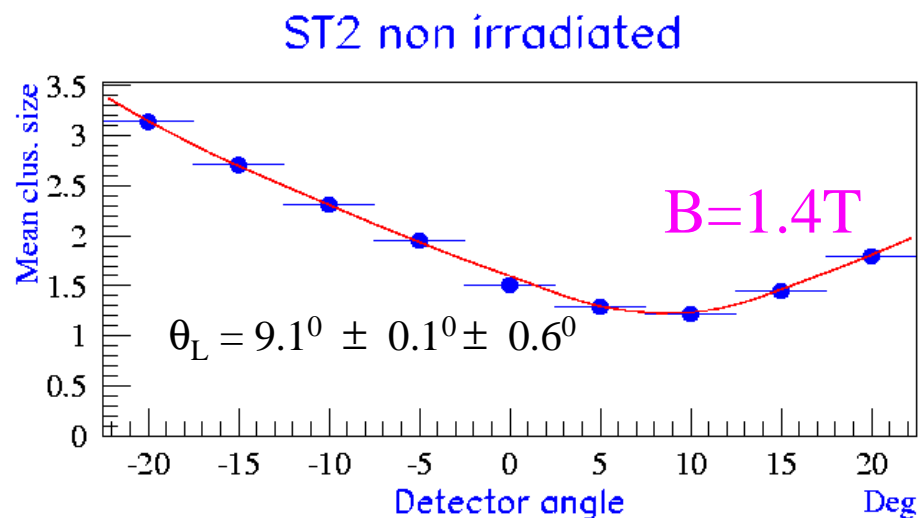


Lorentz Angle



not irradiated $9.1^\circ \pm 0.1^\circ \pm 0.6^\circ$
 dose 5×10^{14} n/cm² $3.0^\circ \pm 0.5^\circ \pm 0.2^\circ$
 dose 10^{15} n/cm² $3.2^\circ \pm 1.2^\circ \pm 0.5^\circ$

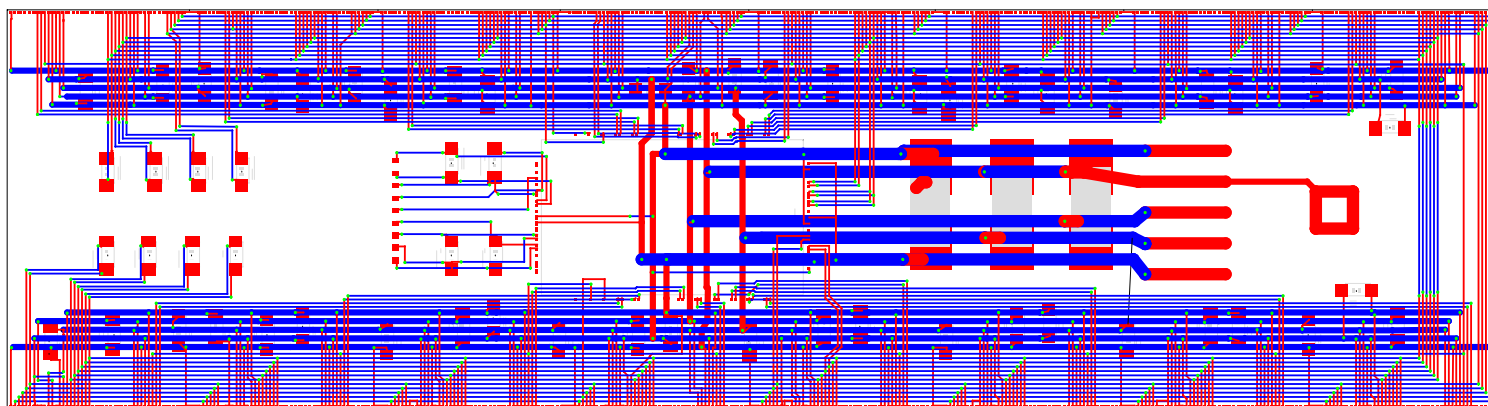
The irradiated results are not understood
 Has impact on overall charge collection in
 barrel region since modules are tilted
 wrt to radial ray





Pixel Hybrids

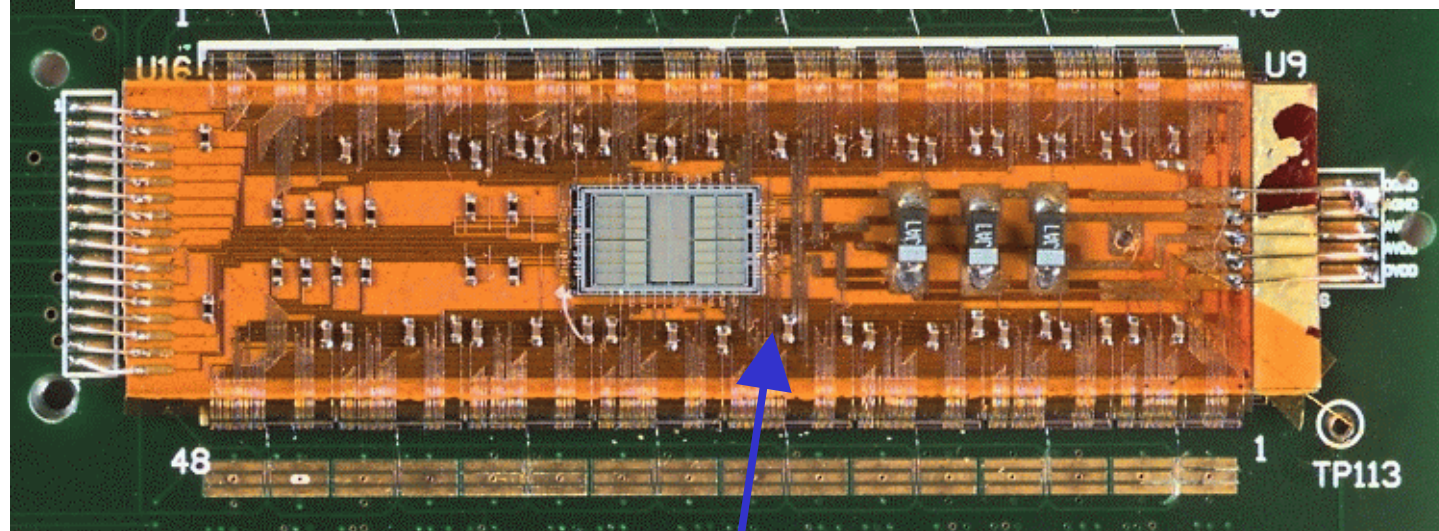
- Flex hybrid interconnect technology selected February 1999 as baseline for disks and two outer barrel layers. B-layer alternative technology(MCM-D) if it proves to be feasible, otherwise flex hybrid.
- Prototype flex hybrid(v1.0) designed at Oklahoma and fabricated successfully at CERN
- Few modules built and tested successfully.
- Design of revised and improved version(1.x) complete. Fabrication complete at CERN and underway in alternative U.S. vendor.



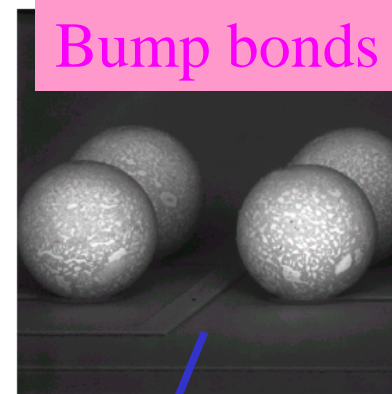


Pixel Modules

Module with flex hybrid and controller chip on PC board



Bump bonds



16 chips with 46,000 bump bonds

Xray of bumps

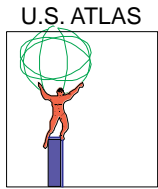


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Sensor

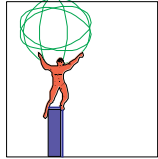
ICs

July 21, 1999



Pixel Modules

- Bump bonding under control for prototypes but much more work needed on production issues.
- A handful of modules(including bare modules) built and tested
- So far has been largely test bed for electronics and concept(can you operate 16 chips on a sensor? Yes)
- Issue - production aspects => contracts in place to build 100 module over next year.
- Production planning underway but many, many details to be finalized.
- Prototype production tooling design for module assembly just started last month.



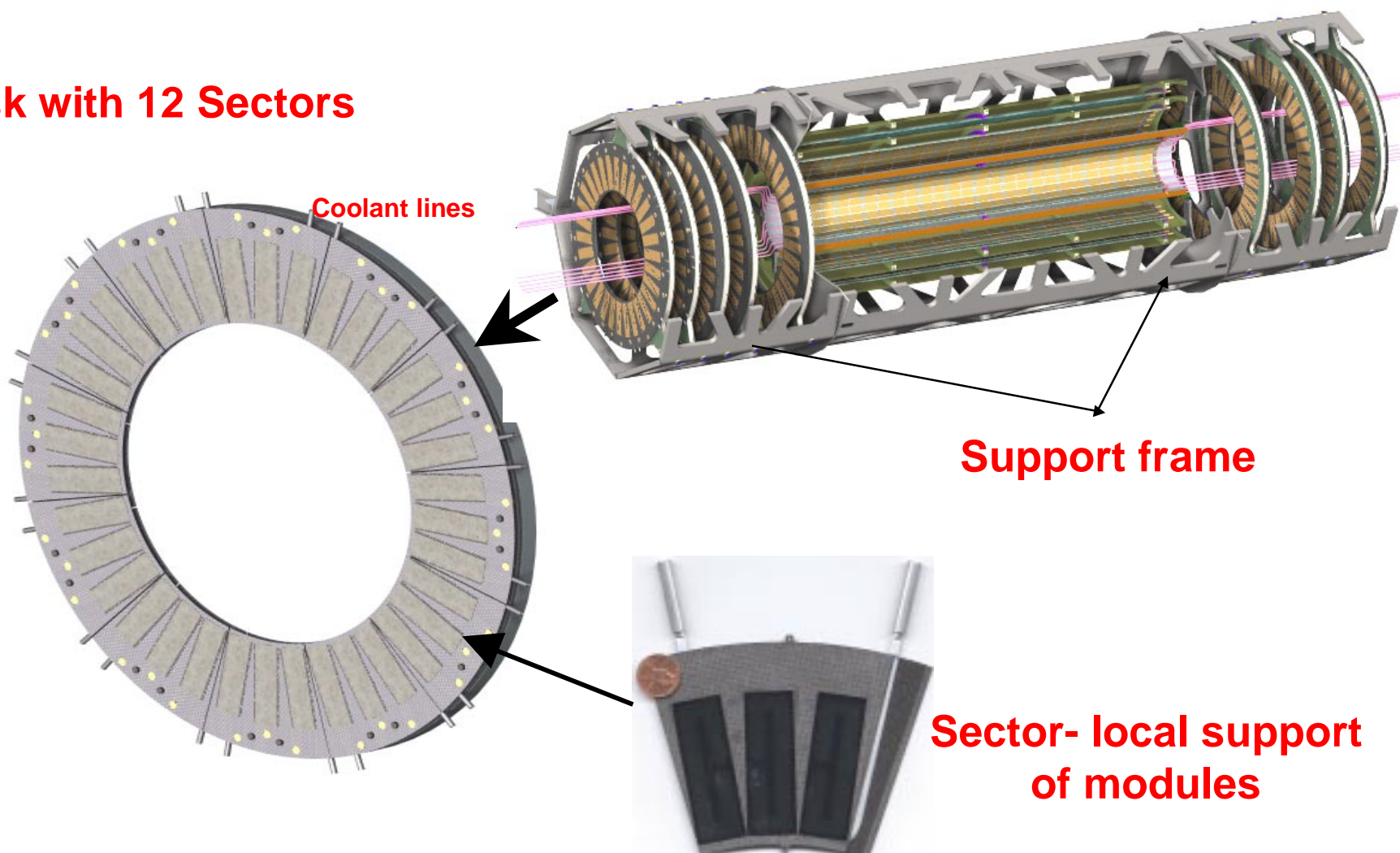
U.S. Pixel Module Production

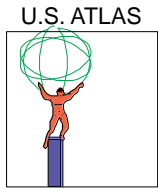
<u>FE ICs</u>		<u>Detectors</u>		<u>Flex Hybrid</u>			
Fab	LBL	Fab	New Mexico	Fab	Oklahoma		
Ship	LBL	Ship	New Mexico	Inspect(in fab)	Oklahoma		
Probe	LBL	Probe	New Mexico	Ship	Oklahoma		
Ship	LBL	Ship	New Mexico	Cut(in fab)	Oklahoma		
Bump deposition		Bump deposition		Ship	Oklahoma		
Ship		Ship		Probe(in fab)	Albany		
Inspection(bump yield)		Inspection(bump yield)		Ship	Albany		
Ship		Ship		Mount components	Oklahoma		
Thin and metallize	LBL, if needed	Dice		Ship	Oklahoma		
Ship	LBL, if needed	Sort		Wire bond	LBL		
Dice	LBL, if needed	Ship		Ship	LBL		
Sort	LBL, if needed	Inspect		Probe/burn-in	Albany, Oklahoma/LBL, if needed		
Ship	LBL, if needed			Ship	Albany, Oklahoma/LBL, if needed		
Inspect	LBL, if needed						
<u>Optical Components</u>		<u>Module Assembly</u>		<u>Local Power Cabling</u>			
IC fab	Ohio	Flip chip/die		Fab	LBL		
IC Ship	Ohio	Flip chip/module		Inspect/Test	LBL		
IC Probe	Ohio	Ship		Ship	LBL		
IC Ship	Ohio	Inspect					
IC thin	Ohio, LBL if needed	Ship		<u>MCC ICs</u>			
IC dice	Ohio, LBL if needed	Probe bare module	LBL	Fab			
IC Ship	Ohio, LBL if needed	Ship	LBL	Ship			
Fiber fab	Ohio	Attach flex	LBL, others are TBD	Probe			
Fiber ship	Ohio	Wire bond(with repair)	LBL, others are TBD	Ship			
Fiber inspect/test	Ohio	Attach pwr/optics	LBL, others are TBD	Thin	LBL, if needed		
Package fab	Ohio	Ship	LBL, others are TBD	Ship	LBL, if needed		
Package ship	Ohio	Test/burn in	Albany, UNM, OSU, UOK	Dice	LBL, if needed		
Package inspect/test	Ohio	Ship	Albany, UNM, OSU, UOK	Ship	LBL, if needed		
Package ship	Ohio						
		<u>Database</u>					
		Requirements	LBL, New Mexico				
		Code development	LBL, New Mexico				
		Central hardware					
		Code support	LBL				



Pixel Mechanics

Disk with 12 Sectors





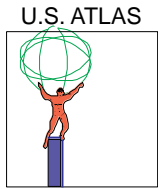
Pixel Mechanics - Status

- **Sectors**

- ◆ About one dozen prototypes tested
- ◆ Baseline is all-carbon design fabricated by ESLI in San Diego and developed via SBIR funding
- ◆ However, have developed full in-house backup to mitigate sole source and technical risk. Additional all-carbon backup also being developed via SBIR funding
- ◆ Extensive test program
 - ▲ Thermal performance(IR and temperature measurements)
 - ▲ Mechanical stability(TV holography and optical CMM)
 - ▲ Irradiated full prototype to 22 Mrad. Nearly same performance

- **Disks**

- ◆ Prototype support ring fabricated
- ◆ ESLI is producing >12 sectors to make full disk
- ◆ Full tests using TV holography and at LBNL using CMMs
- ◆ 2nd disk prototype by fall of this year



Pixel Mechanics - Status

- **Support structure**

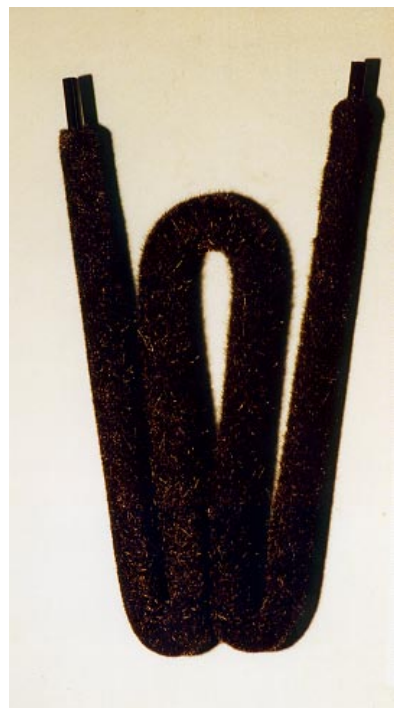
- ◆ Conceptual design completed by Hytec, Inc for Technical Design Report and was funded by US, Italy and Germany
- ◆ Agreement in last few months on splitting prototype design and fabrication between US(overall frame and disk region) and Europe(barrel shells)
- ◆ Full-scale prototype of one disk region designed by Hytec, Inc
- ◆ Contract with fabrication vendor in place. Materials delivered or ordered. Fabrication started. Three phase program, ending in complete prototype by end of year.

- **Integration**

- ◆ Interfaces, power and signal cabling, cooling, installation conceptual framework developed for all integration issues
- ◆ 3D modeling and multiple physical models(complete end region at LBNL and partial region in UK as part of overall ID) underway.
- ◆ This is a major effort.....

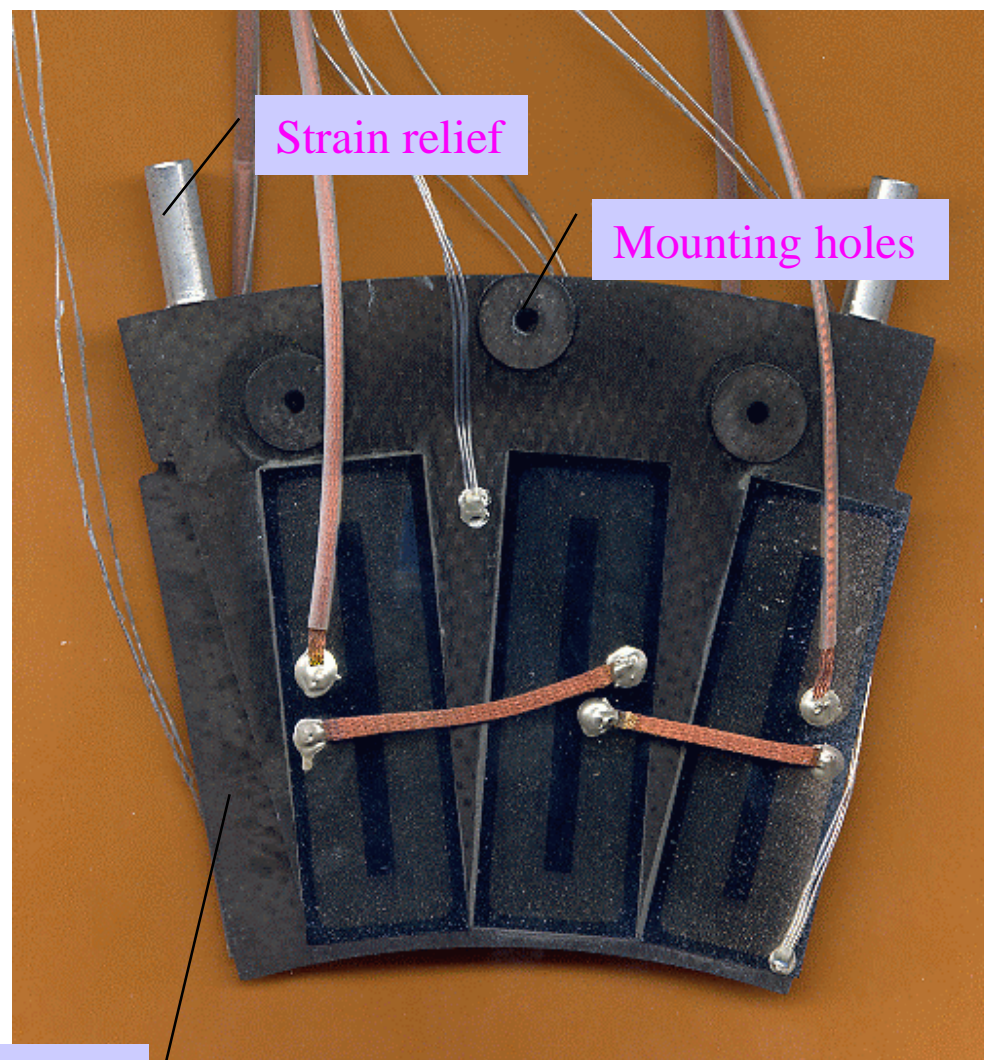


All-Carbon Sector

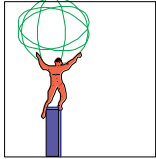


Leak tight carbon tube flocked with high thermal conductivity fibers.

300-500 micron carbon-carbon facings



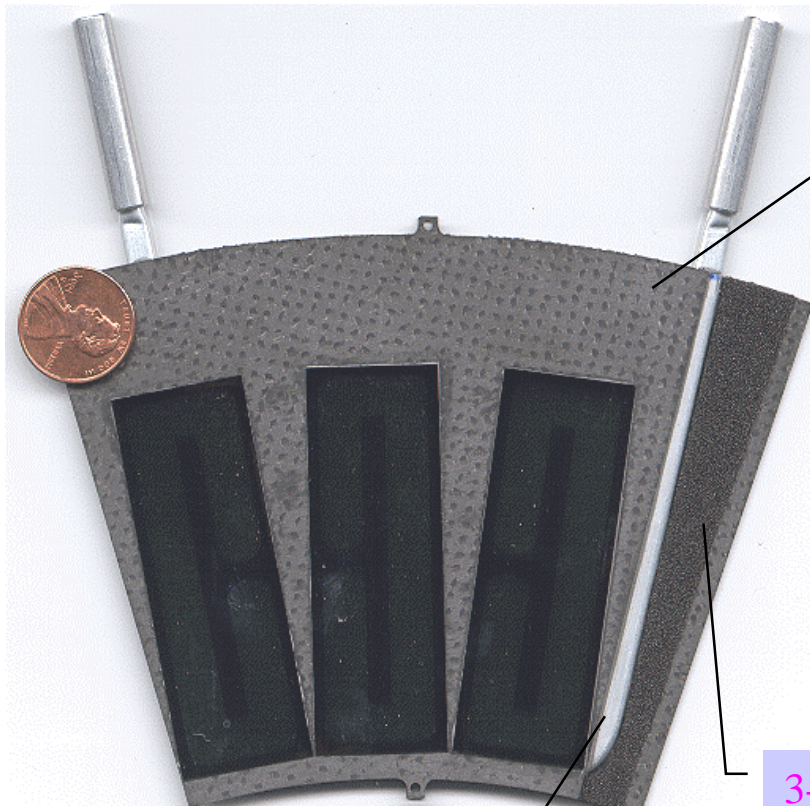
July 21, 1999



Al-Tube Sector

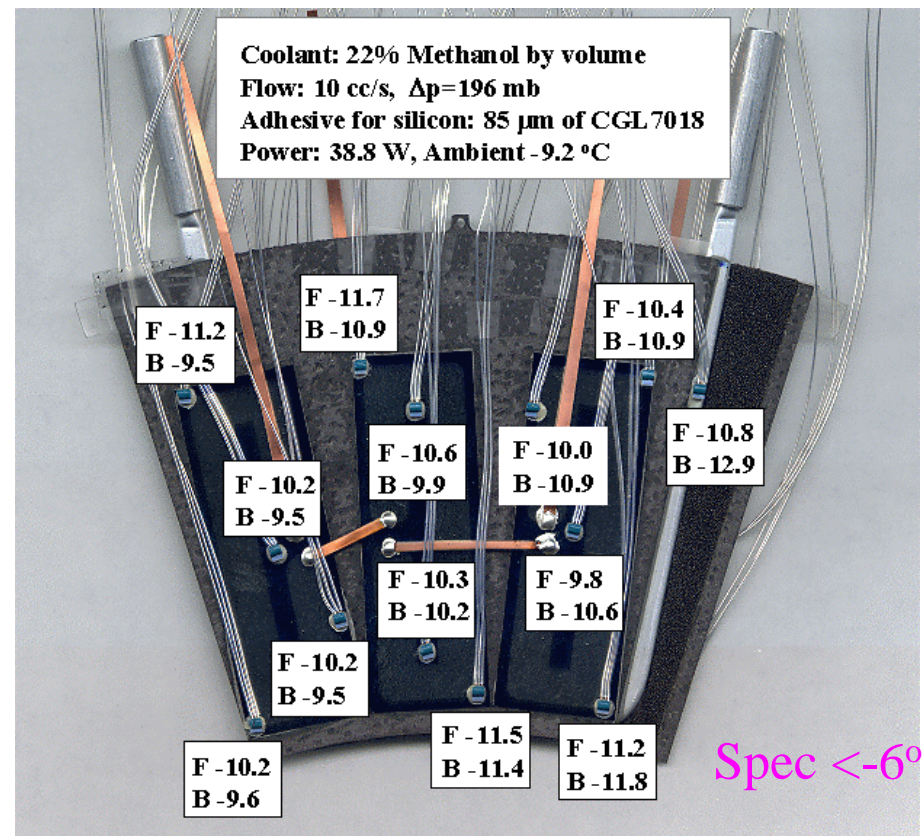
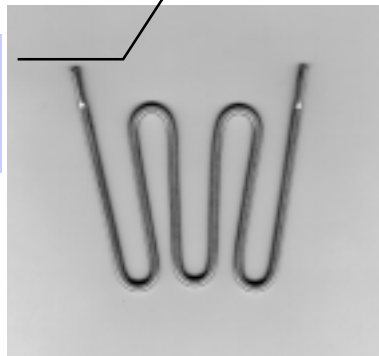
LBNL design and fabrication

300-500 micron carbon-carbon facings



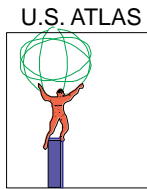
200 micron wall Al tube

3-6% density carbon foam



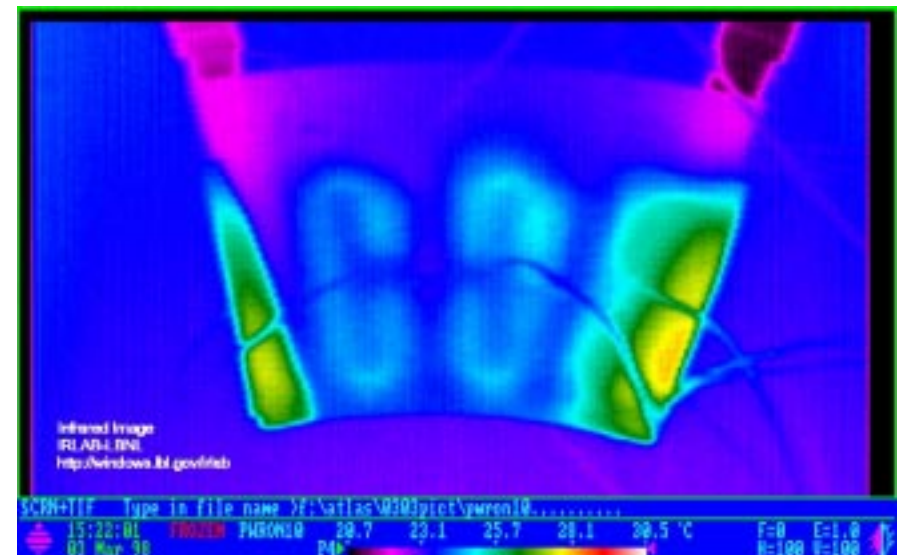
Spec $< -6^\circ$

July 21, 1999

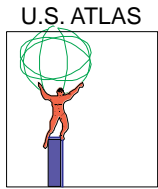


Thermal Measurements and Cooling

- In addition to direction temperature measurements, also use infrared imaging.
- Have used water-methanol, liquid C_6F_{14} and evaporative fluorocarbons (C_4F_{10} and others).
- All can work thermally but water-based rejected (risk) and liquid fluorcarbon rejected (so far) because more material.
- Baseline cooling is evaporative. First tests show it works but much development needed at system level



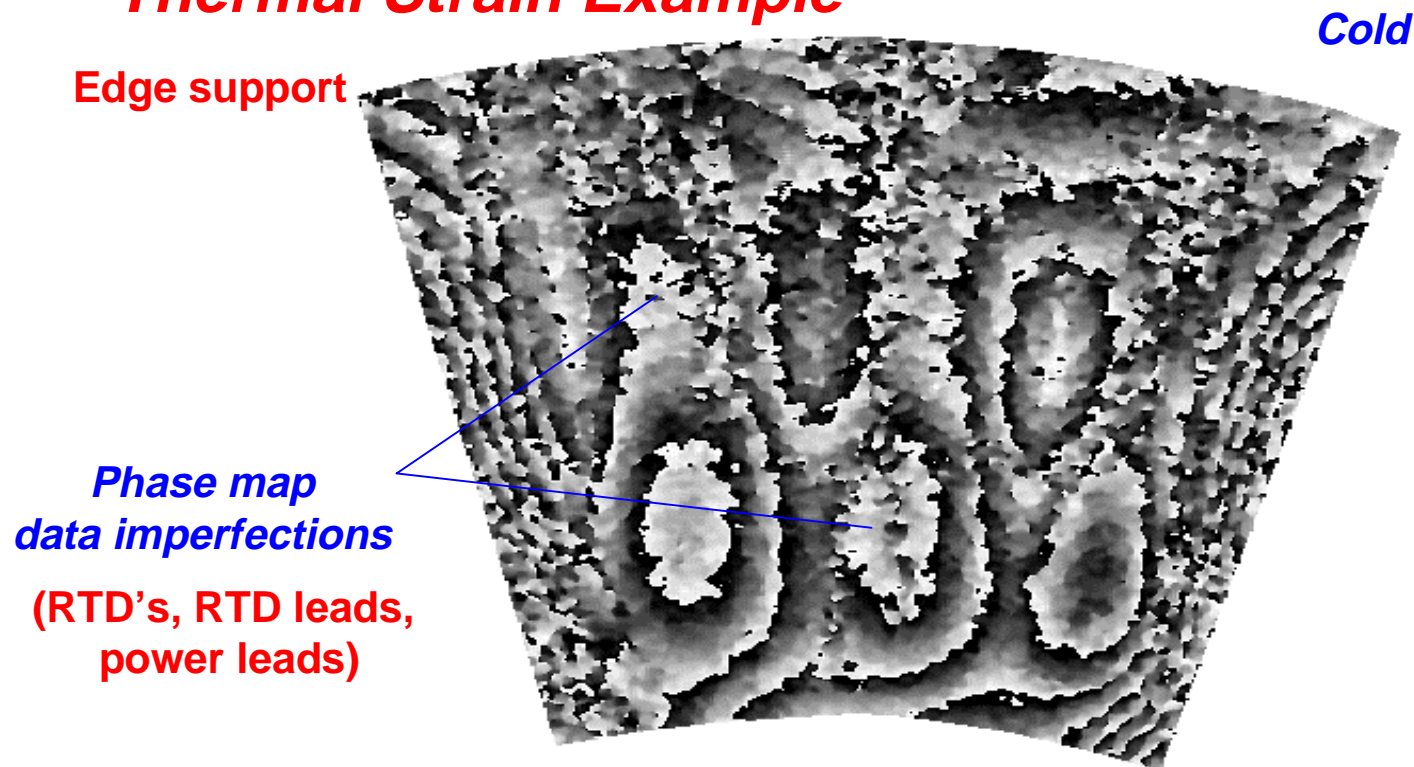
July 21, 1999



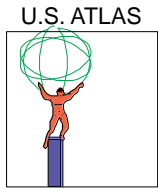
Mechanical Stability Measurements

- Trying for ultra-stable structure
- Validate using TV holography(<1 micron precision) and with direct optical CMM measurements

Thermal Strain Example

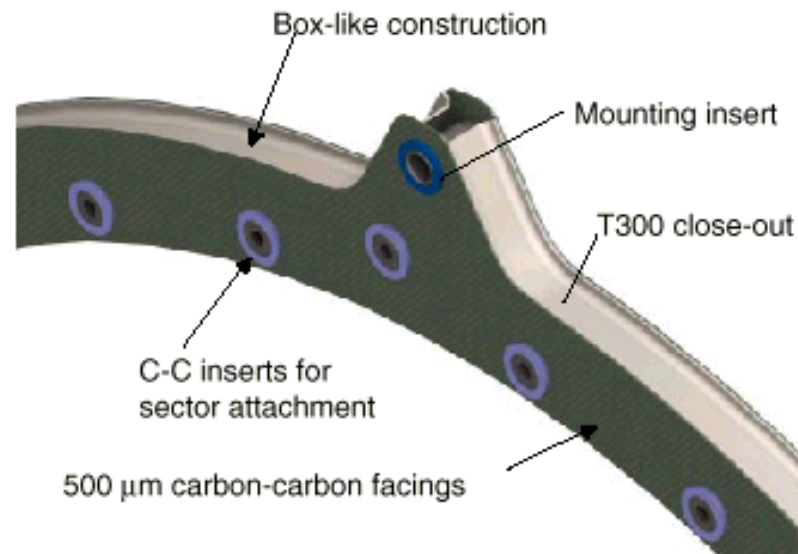
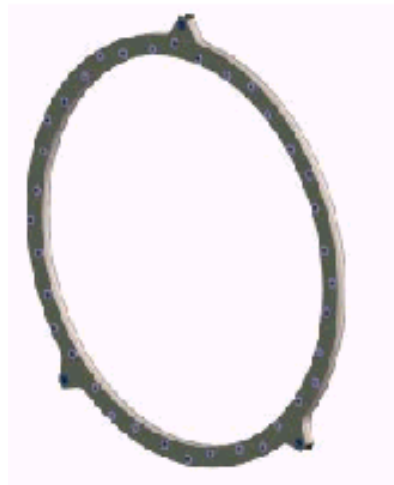


$\Delta T = 1.1 \text{ }^{\circ}\text{C}$ @ $T = -15.3 \text{ }^{\circ}\text{C}$
 $\sim 2 \text{ } \mu\text{m}$'s peak out-of-plane



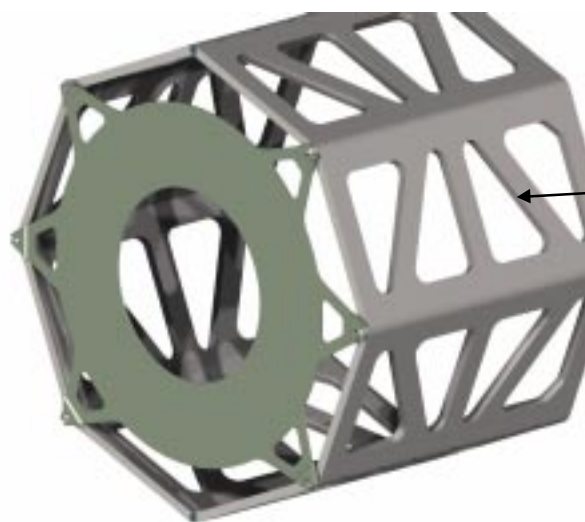
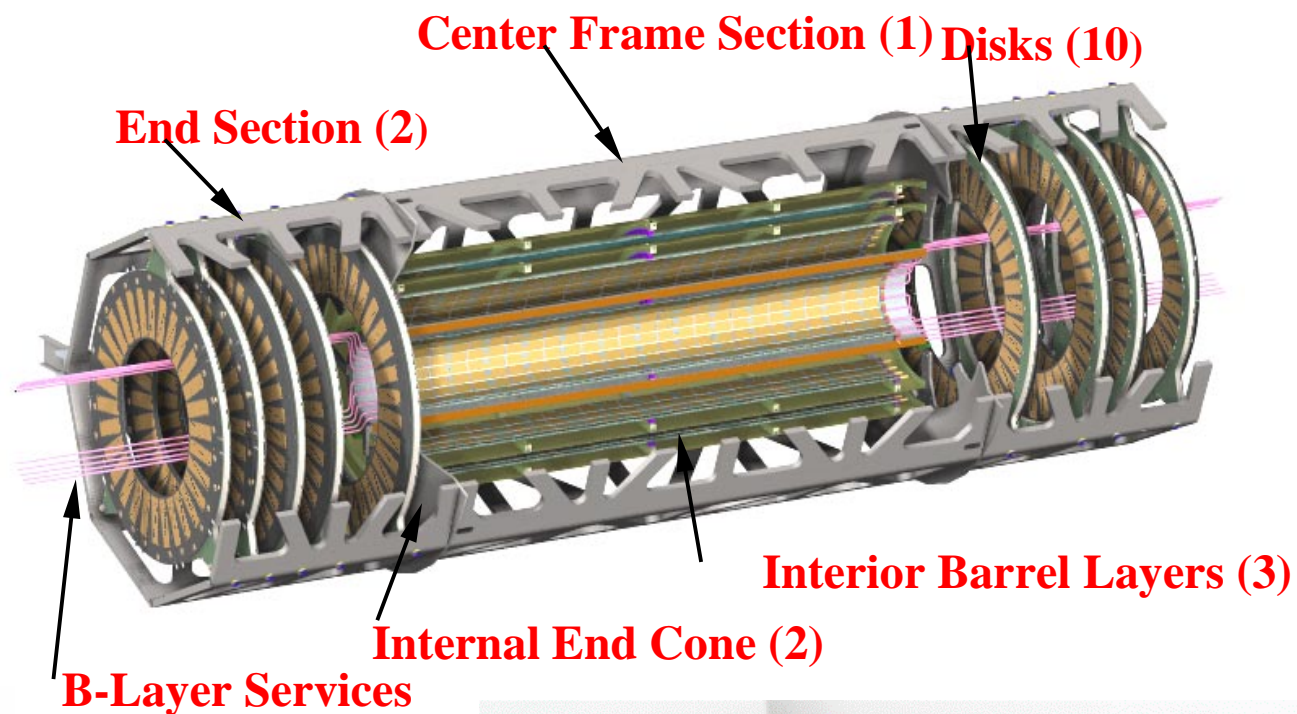
Disk Prototype

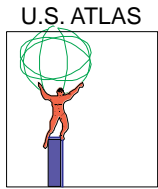
- Two full-disk prototypes will be made
- Fabrication of first one is nearing completion (sectors from ESLI) and disk support ring





Prototype Frame Started





Conclusion

- **ROD prototype by early next year.**
- **Revised SCT electronics being tested or soon to be tested. If OK, then onward to (pre)production and module construction.**
- **Tremendous progress in developing pixel technology. This must work for ATLAS and so far it can.**